EXHIBIT 3

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; and MICRON TECHNOLOGY TEXAS LLC,
Petitioners,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2021-00745
U.S. Patent No. 10,489,314

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 10,489,314

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TABLE OF ABBREVIATIONS AND CONVENTIONS

Abbreviation	Meaning
Decl.	Declaration of Dr. Vojin Oklobdzija (Ex. 1003)
Halbert	U.S Patent Application Publication No. 2002/0112119 to Halbert et al. (Ex. 1005)
JESD21-C	PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification, JEDEC Standard 21-C (January 2002) (Ex. 1006)

PETITIONER'S EXHIBIT LIST

Ex. No.	Brief Description
1001	U.S. Patent No. 10,489,314
1002	File History of U.S. Patent No. 10,489,314
1003	Declaration of Dr. Vojin Oklobdzija
1004	Curriculum Vitae of Dr. Vojin Oklobdzija
1005	U.S Patent Application Publication No. 2002/0112119 to Halbert et al.
1006	PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification, JEDEC Standard 21-C (January 2002)
1007	RESERVED
1008	Netlist Proposed Claim Construction in *Netlist, Inc. v. Micron Technology, Inc. et al.*, Case No. 6:21-cv-00431 (W.D. Tex.)
1009	Micron's Proposed Claim Construction in *Netlist, Inc. v. Micron Technology, Inc. et al.*, Case No. 6:21-cv-00431 (W.D. Tex.)
1010	Defendants' Stipulation of Invalidity Contentions for U.S. Patent No. 10,489,314, *Netlist, Inc. v. Micron Technology, Inc. et al.*, Case No. 1:22-cv-00136 (W.D. Tex.)
1011	Pre-*Markman* Scheduling Order, *Netlist, Inc. v. Micron Technology, Inc. et al.*, Case No. 1:22-cv-00136 (W.D. Tex.)

CLAIM LISTING

Ref. No.	Listing of Challenged Claims
Limitation [15.1]	A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory module comprising:
Limitation [15.2]	a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;
Limitation [15.3]	logic coupled to the printed circuit board and configured to receive a first set of input address and control signals associated with a first read or write memory command and to output a first set of registered address and control signals in response to the first set of input address and control signals,
Limitation [15.4]	the first set of input address and control signals including a first plurality of input chip select signals,
Limitation [15.5]	the first set of registered address and control signals including a first plurality of registered chip select signals corresponding to respective ones of the first plurality of input chip select signals,
Limitation [15.6]	the first plurality of registered chip select signals including a first registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value;
Limitation [15.7]	memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks are configured to receive respective ones of the first plurality of registered chip select signals,

Ref. No.	Listing of Challenged Claims
Limitation [15.8]	wherein a first N-bit wide rank in the plurality of N-bit wide ranks receiving the first registered chip select signal having the active signal value is configured to receive or output a first burst of N-bit wide data signals and a first burst of data strobes associated with the first read or write command;
Limitation [15.9]	circuitry coupled between data and strobe signal lines in the N-bit wide memory bus and corresponding data and strobe pins of memory devices in each of the plurality of N-bit wide ranks; and
Limitation [15.10]	wherein the logic is further configured to, in response to the first read or write memory command, output first control signals to the circuitry,
Limitation [15.11]	and wherein the circuitry is configured to enable data transfers between the first rank and the memory bus through the circuitry in response to the first control signals so that respective N-bit wide data signals of the first burst of N-bit wide data signals and respective data strobes of the first burst of data strobes are transferred through the circuitry in accordance with an overall CAS latency of the memory module; and
Limitation [15.12]	wherein the data transfers between the first rank and the memory bus through the circuitry are registered data transfers and the circuitry is configured to add a predetermined amount of time delay for each registered data transfer through the circuitry such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.
Limitation [16.1]	The memory module of claim 15, wherein each of the memory devices has a corresponding load,
Limitation [16.2]	the circuitry is configured to isolate the loads of the memory devices from the memory bus.

Ref. No.	Listing of Challenged Claims
Limitation [17.1]	The memory module of claim 15, wherein the first burst of N-bit wide data signals includes a set of consecutively transmitted data bits for each data signal line in the memory bus,
Limitation [17.2]	and wherein the set of consecutively transmitted data bits are successively transferred through the circuitry in response to the first control signals.
Limitation [18.1]	The memory module of claim 15, wherein each of the memory devices is 4-bits wide,
Limitation [18.2]	and wherein each of the plurality of ranks is 72-bits wide and includes 18 memory devices configured in pairs, and wherein each pair of 4-bit-wide memory devices are configured to simulate an 8-bit-wide memory device.
Claim 19	The memory module of claim 15, wherein the memory devices are organized in four ranks and the first set of input address and control signals include four chip select signals, one for each of the four ranks.
Claim 20	The memory module of claim 15, wherein the circuitry includes logic pipelines configured to enable the data transfers between the first rank and the memory bus through the circuitry in response to the first control signals.
Claim 22	The memory module of claim 15, wherein the first burst of N-bit wide data signals and the first burst of data strobes are transferred between the first N-bit wide rank and the memory controller at a specified data rate.
Limitation [23.1]	The memory module of claim 15, further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller,
Limitation [23.2]	wherein the predetermined amount of time delay is at least one clock cycle time delay.

Ref. No.	Listing of Challenged Claims
Limitation [24.1]	The memory module of claim 23, wherein the memory devices are dynamic random access memory devices configured to operate synchronously with the clock signal,
Limitation [24.2]	and wherein each memory device in the first rank is configured receive or output a respective set of bits of the first burst of N-bit wide data signals on both edges of each of a respective set of data strobes of the first burst of data strobes.
Limitation [25.1]	The memory module of claim 15, wherein the logic is further configured to respond to a second set of input address and control signals associated with a second read or write memory command by outputting a second set of registered address and control signals,
Limitation [25.2]	the second set of input address and control signals including a second plurality of input chip select signals,
Limitation [25.3]	the second set of registered address and control signals including a second plurality of registered chip select signals corresponding to respective ones of the second plurality of input chip select signals,
Limitation [25.4]	the second plurality of registered chip select signals including a second registered chip select signal having the active signal value and one or more other registered chip select signals each having the non-active signal value,
Limitation [25.5]	wherein a second rank different from the first rank is configured to receive the second registered chip select signal having the active signal value and to output or receive a second burst of N-bit wide data signals and a second burst of data strobes associated with the second read or write command,
Limitation [25.6]	wherein the logic is further configured to, in response to the second read or write memory command, output second control signals to the circuitry,

Ref. No.	Listing of Challenged Claims
Limitation [25.7]	and wherein the circuitry is configured to enable registered data transfers between the second rank and the memory bus through the circuitry in response to the second control signals so that the second burst of N-bit wide data signals and the second burst of data strobes are transferred between the second rank and the memory controller through the circuitry in accordance with the overall CAS latency of the memory module.
Limitation [26.1]	The memory module of claim 17, wherein the first burst of N-bit wide data signals is transferred through the circuitry in a plurality of time intervals including at least a first time interval and a last time interval,
Limitation [26.2]	wherein the circuitry includes a set of signal paths that are enabled before the first time interval and subsequently disabled after the last time interval.
Limitation [27.1]	The memory module of claim 26, wherein: the first read or write memory command is a read memory command;
Limitation [27.2]	the second read or write memory command is a write memory command;
Limitation [27.3]	the set of signal paths are enabled to transfer the first burst of N-bit wide data signals and the first burst of data strobes a first number of time intervals after the read memory command is received by the logic; and
Limitation [27.4]	the set of signal paths are enabled to transfer the second burst of N-bit wide data signals and the second burst of data strobes a second number of time intervals after the write memory command is received by the logic, the second number being different from the first number.
Limitation [28.1]	A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response

Ref. No.	Listing of Challenged Claims
	to read or write memory commands received from the memory controller, the memory module comprising:
Limitation [28.2]	a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;
Limitation [28.3]	logic coupled to the printed circuit board and configured to receive a set of input control and address signals associated with a read or write memory command via the memory bus and to output a set of registered control and address signals in response to the set of input control and address signals,
Limitation [28.4]	the set of input control and address signals including a plurality of input chip select signals,
Limitation [28.5]	the set of registered control and address signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals,
Limitation [28.6]	the plurality of registered chip select signals including a registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value;
Limitation [28.7]	memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks are configured to receive respective ones of the plurality of registered chip select signals,
Limitation [28.8]	wherein a first N-bit wide rank receiving the registered chip select signal having the active signal value is configured to receive or output a first burst of N-bit wide data signals and a first burst of data strobes associated with the read/write command;

Ref. No.	Listing of Challenged Claims
Limitation [28.9]	circuitry between data and data strobe signal lines in the memory bus and corresponding data and data strobe pins of the memory devices,
Limitation [28.10]	wherein the circuitry includes logic pipelines configured to enable data transfers between the first rank and the memory bus in response to the first read or write memory command,
Limitation [28.11]	wherein respective N-bit wide data signals of the first burst of N-bit wide data signals and respective data strobes of the first burst of data strobes are transferred between the first rank and the memory bus through the circuitry in accordance with an overall CAS latency of the memory module; and
Limitation [28.12]	wherein the data transfers between the first rank and the memory bus are registered data transfers; and
Limitation [28.13]	wherein the circuitry is configured to add a predetermined amount of time delay for each data transfer between the memory controller and the memory devices such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.
Limitation [29.1]	The memory module of claim 28, wherein the first burst of N-bit wide data signals includes a set of consecutively transmitted data bits for each data signal line in the memory bus,
Limitation [29.2]	and wherein the circuitry includes a set of signal paths that are enabled before a first data bit of the set of consecutively transmitted data bits is transferred through the circuitry and disabled after a last data bit of the set of consecutively transmitted data bits is transferred through the circuitry.
Limitation [30.1]	The memory module of claim 28, wherein the logic is further configured to respond to a subsequent set of input address and control signals associated with a subsequent

Ref. No.	Listing of Challenged Claims
	read or write memory command by outputting a subsequent set of registered address and control signals,
Limitation [30.2]	the subsequent set of input address and control signals including a subsequent plurality of input chip select signals,
Limitation [30.3]	the subsequent set of registered address and control signals including a subsequent plurality of registered chip select signals corresponding to respective ones of the subsequent plurality of input chip select signals,
Limitation [30.4]	the subsequent plurality of registered chip select signals including a subsequently registered chip select signal having the active signal value and one or more other subsequently registered chip select signals each having the non-active signal value,
Limitation [30.5]	wherein a second rank different from the first rank is configured to receive the subsequently registered chip select signal having the active signal value and to output or receive a second burst of N-bit wide data signals and a second burst of data strobes associated with the subsequent read or write command,
Limitation [30.6]	wherein the circuitry is further configured to enable registered data transfers between the memory devices and the memory bus in response to the subsequent read/write memory command so that the second burst of N-bit wide data signals and the second burst of data strobes are transferred between the second rank and the memory bus through the circuitry.
Claim 31	The memory module of claim 28, wherein the first burst of N-bit wide data signals and the first burst of data strobes are transferred between the first N-bit wide rank and the memory controller at a specified data rate.
Limitation [32.1]	The memory module of claim 28, further comprising a phase locked loop clock driver configured to output a clock

Ref. No.	Listing of Challenged Claims
	signal in response to one or more signals received from the memory controller,
Limitation [32.2]	wherein the predetermined amount of time delay is at least one clock cycle time delay.
Limitation [33.1]	The memory module of claim 32, wherein the memory devices are dynamic random access memory devices configured to operate synchronously with the clock signal,
Limitation [33.2]	and wherein each memory device in the first rank is configured receive [*sic*] or output a respective set of bits of the first burst of N-bit wide data signals on both edges of each of a respective set of data strobes of the first burst of data strobes.

I. Introduction

Petitioners Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC ("Petitioners"/"Micron") request *inter partes* review ("IPR") of claims 15-20 and 22-33 ("Challenged Claims") of U.S. Patent No. 10,489,314 ("'314 patent").

The '314 patent is generally directed to a memory module[1] that is connectable to a computer's memory controller. The memory module includes ranks of memory devices[2] and register buffers that separate the memory devices from the connections to the memory controller. The patent observes that the addition of register buffers will add a clock cycle time delay that results in a memory module with an overall Column Address Strobe ("CAS") latency ("CL") greater than the actual operational CL of the memory devices.

The fatal flaw to the Challenged Claims is that memory modules as claimed were well-known. For example, U.S. Patent Application Publication No. 2002/0112119 to Halbert et al. ("Halbert") discloses a very similar memory module with ranks of memory devices separated from a memory controller by register

[1] For example, a dual in-line memory module ("DIMM") card.

[2] For example, dynamic random access memory ("DRAM") cells.

buffers. Indeed, the Board in IPR2017-00549 relied upon Halbert to find challenged claims in the '314 patent's extended family unpatentable.

As explained in this Petition, the Challenged Claims would not have been allowed if Halbert had been substantively evaluated by the Examiner during prosecution of the '314 patent. The Challenged Claims are unpatentable and should be cancelled.

II. Requirements for *Inter Partes* Review

This Petition complies with all statutory requirements, as well as 37 C.F.R. §§ 42.104, 42.105, and 42.15, and should be accorded a filing date pursuant to 37 C.F.R. § 42.106. The required fee is being paid electronically through PTAB E2E.

A. The '314 Patent is Available for *Inter Partes* Review

As required by 37 C.F.R. § 42.104(a), Petitioners certify that the '314 patent "is available for *inter partes* review and that the Petitioners are not barred or estopped from requesting an *inter partes* review challenging the patent claims on the grounds identified in the petition." Petitioners certify that this Petition is filed within one year of the date of service of the complaint—June 15, 2021—where Netlist alleged infringement of the '314 patent. No Petitioner, nor any party in privity with Petitioners, has filed a civil action challenging the validity of any claim of this patent.

B. Ground

Under 37 C.F.R. §§ 42.104(b) and 42.22, Petitioners request that the Board institute this IPR on claims 15-20 and 22-33 of the '314 patent and cancel those

claims as unpatentable for obviousness under pre-AIA 35 U.S.C. § 103 on the following ground:

Ground	Claim	Basis for Unpatentability
1	15-20 and 22-33	Halbert in view of JEDEC Standard 21-C

III. The '314 Patent

A. Earliest Effective Filing Date

The '314 patent claims priority through a series of applications, the earliest being provisional application No. 60/550,668, filed on March 5, 2004. For purposes of this Petition, Petitioners assume an effective filing date of March 5, 2004.

B. Level of Ordinary Skill in the Art

As of March 2004, a person of ordinary skill in the art ("POSITA") would have been someone with an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working the field. Decl., ¶ 52. Such a person would have been knowledgeable about the design and operation of computer memories, most particularly DRAM and SDRAM devices that were compliant with various standards of the day, and how they interact with other components of a computer system, such as memory controllers. *Id*. He or she would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs and CPLDs and

less sophisticated circuits such as tri-state buffers, flip flops, and registers. *Id*. The references cited in this Petition and the experience of Dr. Vojin Oklobdzija, as described in his expert declaration, reflect this level of skill in the art.

C. Overview of the '314 Patent

The '314 patent relates to memory modules that are described in terms of single in-line memory modules ("SIMMs"), DIMMs, and other types of memory cards of various sizes. Ex. 1001, 6:14-23, 6:31-38. The memory modules are described as a "printed circuit board" containing "edge connectors" for coupling to a "module slot of a computer system." *Id.*, 6:25-28. The memory modules communicate with a host computer's "memory controller" through this module slot and via a "data bus." *Id.*, 3:17-20.

The memory modules include "memory devices," such as random access memory, DRAM, and other types of commercially available devices. *Id.*, 6:39-58. The modules are arranged in ranks. For example, Fig. 9B depicts two ranks (32a-32b), and Fig. 9A depicts four ranks (32a-32d):

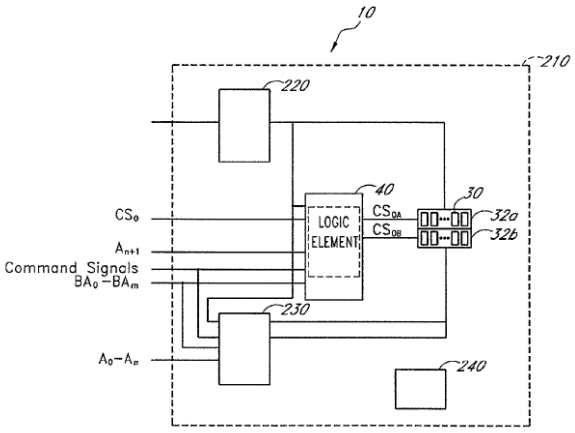


FIG. 9B

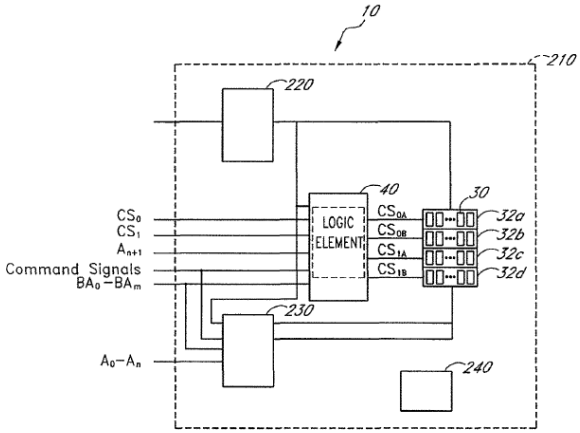


FIG. 9A

Id., Figs. 9A-9B.

As depicted in Figs. 9A-9B, the memory devices are coupled to "circuit" 40 and "register" 230. Circuit 40 "receives a set of input address and command signals" and "generates a set of output address and command signals in response." *Id.*, 16:27-32. Register 230 "receives and buffers a plurality of command signals and address signals." *Id.*, 16:45-46. Also depicted is "SPD" 240, which communicates data regarding various attributes of the memory module to the "basic input/output (BIOS) of the computer system so that the computer system is informed of the memory capacity." *Id.*, 19:36-47.

The '314 patent describes an embodiment where the SPD "reports a CL which has one more cycle than does the actual operational CL of the memory devices." *Id.*, 22:41-43. This SPD reporting feature is described in terms of the one clock cycle delay caused by transferring data through a register buffer included between the

module's memory devices and its connections to the host memory controller. *Id.*, 22:43-62

D. Relevant Prosecution History of the '314 Patent Family

No office action rejections were issued during prosecution of the '314 patent. The Halbert and JEDEC Standard 21-C ("JESD21-C") references relied upon herein were identified on an IDS form by Netlist during prosecution. Neither were substantively addressed, or even discussed, by the Examiner. Both references, however, were substantively evaluated by the Board in IPRs that found claims in the '314 patent's family unpatentable.[3]

IV. Claim Construction

The Board construes claims under the same standard used in civil actions in federal district court. 37 C.F.R. § 42.100(b). The district court for the related litigations has not yet construed the claim terms. The parties' proposed constructions from those actions are set forth in Exs. 1008-1009.

[3] The Board examined Halbert in IPR2017-00549 and JESD21-C in IPR2014-00883, IPR2015-01021, and IPR2015-01020. The challenged patents in these proceedings (U.S. Patent Nos. 8,756,364, 8,081,536, and 7,881,150) and the '314 patent challenged herein all claim priority to provisional Application Nos. 60/550,668, 60/575,595, and 60/590,038; and U.S. Patent Nos. 7,289,386 and 7,286,436.

The parties' construction disputes from the related litigations do not affect the outcome of this Petition with respect to any claim.

First, for the terms "overall CAS latency …" and "actual operational CAS latency …," the prior art invalidates the claims under either side's proposed constructions, as shown herein. Petitioners' analysis identifies how the claims are invalid under both Petitioners' and Netlist's proposed constructions for these terms. Second, with respect to the terms that Petitioners contend are indefinite in the related litigations, Petitioners use Netlist's "plain meaning" interpretations herein. To be clear, Petitioners are not asking the Board to find any claim indefinite for the purposes of this Petition. The Board and Federal Circuit have approved of this procedure in several matters. *See, e.g., Micron Tech., Inc. et al. v. Unification Techs. LLC*, IPR2021-00344, Paper 9 at 10-11 (P.T.A.B. July 9, 2021); *Spherix Inc. v. Matal*, 703 F. App'x 982, 983 (Fed. Cir. 2017) (approving petitioner's proposal of patent owner's claim interpretations); *Target Corp. v. Proxicom Wireless, LLC*, IPR2020-00904, Paper 11 at 12 (P.T.A.B. Nov. 10, 2020) ("Petitioner's alternative pleading before a district court is common practice, especially where it concerns issues outside the scope of *inter partes* review."); *Samsung Elecs. Am., Inc. v. Prisua Eng'g Corp*., 948 F.3d 1342, 1355 (Fed. Cir. 2020); *Vibrant Media v. Gen. Elec. Co*., No. IPR2013-00172, Paper 50, 10 (P.T.A.B. July 28, 2014).

V. Ground for Unpatentability

The Challenged Claims are unpatentable based on one ground. Ground 1 establishes that claims 15-20 and 22-33 are obvious over Halbert in view of JESD21-C. These references and Ground are further discussed below.

A. Overview of the Prior Art

1. Halbert

Halbert is entitled "Dual-Port Buffer-to-Memory Interface." Halbert was filed on March 13, 2002, published on August 15, 2002, and qualifies as prior art under at least pre-AIA 35 U.S.C. § 102(b).

Halbert discloses "a new memory module architecture" for a typical memory system configuration, e.g., shown in Fig. 1 below. Halbert, Abstract, [0004].

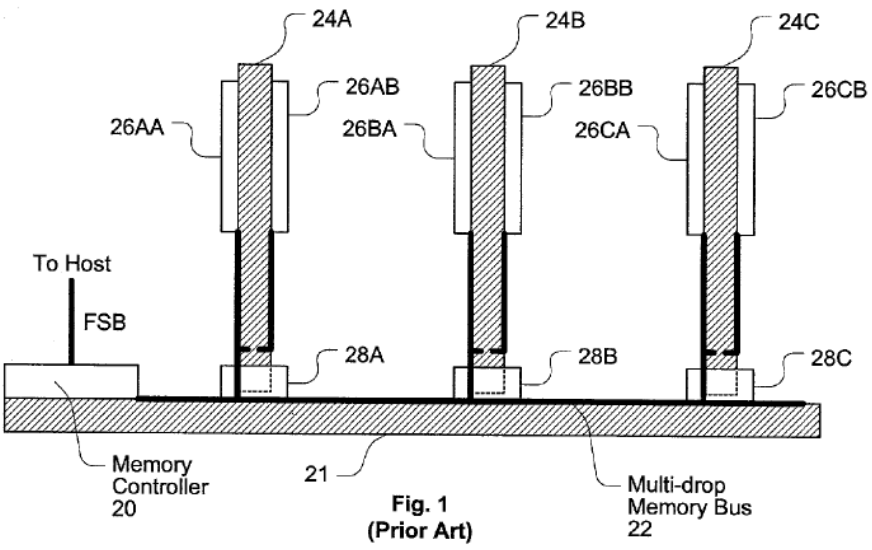


Fig. 1
(Prior Art)

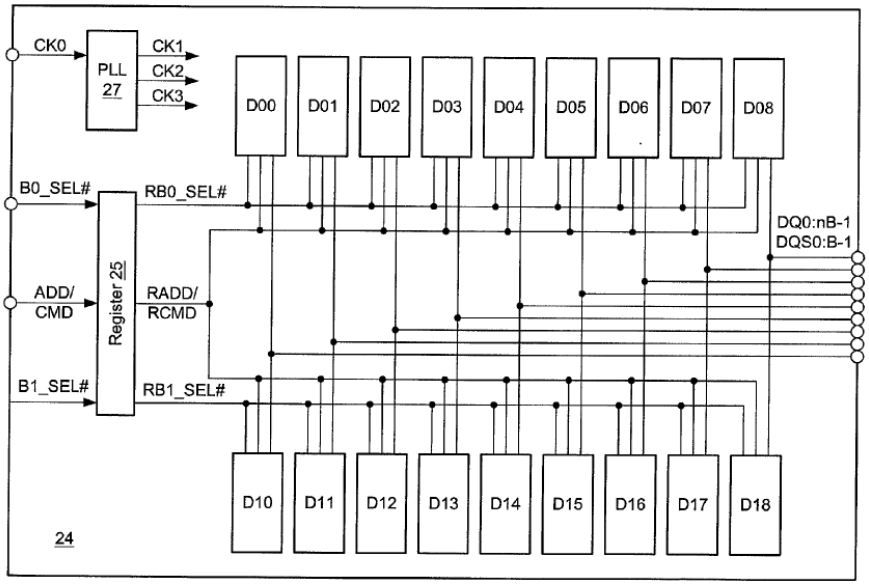
Halbert, Fig. 1.

Halbert's Fig. 1 illustrates an exemplary system with three memory modules 24A-C inserted into corresponding sockets 28A-C and connected to a memory bus

22, which connects to a system memory controller 20. Halbert, [0006]-[0007]. The memory bus 22 carries memory signals, which include "clock and control signals, address signals, command signals, and data signals." *Id*., [0005]; Decl., ¶ 69.

Halbert illustrates an exemplary prior art module, such as "a registered DIMM 24 containing eighteen memory devices arranged in two banks, one containing devices D00-D08 and the other containing devices D10-D18," as shown in Fig. 2 below. Halbert, [0009]; Decl., ¶ 70.

Fig. 2
(Prior Art)



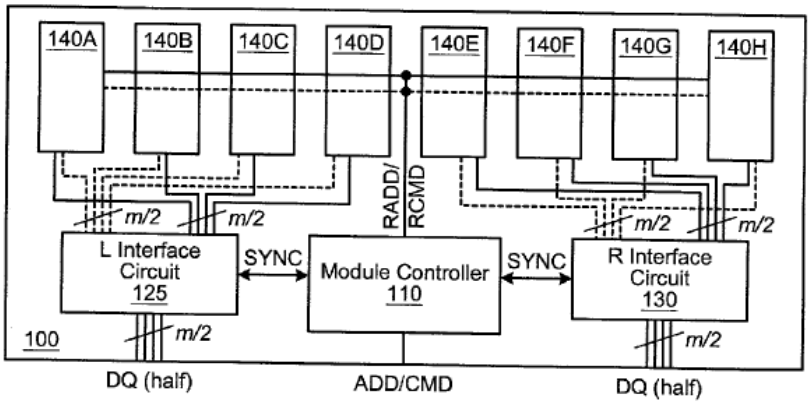
Halbert, Fig. 2.

The prior art DIMM 24 has a register 25 that latches on the address and command signals ADD/CMD and re-drives those signals onto the module's address/command bus connected to the memory devices D00-D18. Halbert, Fig. 2. The register 25 receives bank select signals B0_SEL# and B1_SEL# and provides

registered versions of those signals to chip select pins of corresponding banks of memory devices. *Id.* The data lines from each bank of memory devices are connected to a common set of DQ lines carrying data and DQS lines carrying data strobes. *Id.* Each device has a data width of n (4, 8, or 16) bits that add up to the total of n*B data lines, where B is the number of memory devices per bank (nine in Fig. 2). This prior art module has data lines directly connecting the memory chips to memory bus 22. *Id.*; Decl., ¶ 71.

Halbert discloses a new module architecture that can be implemented to be "transparent to the memory system and to the memory devices … [which] allows for an embodiment that is compatible with an existing memory controller/bus and with existing memory devices." Halbert, [0023]. An exemplary implementation of Halbert's inventive module is shown in Figs. 7-8 below. Decl., ¶ 72.

Fig. 7



Halbert, Fig. 7.

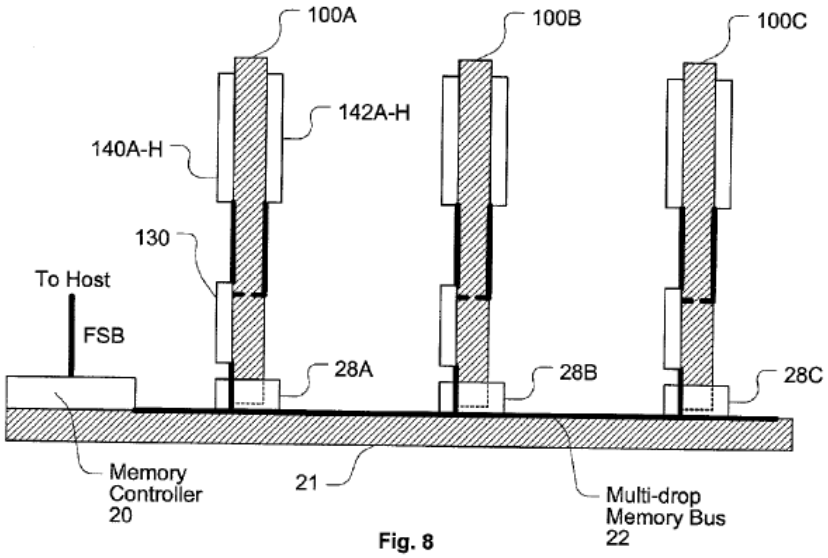


Fig. 8

Id., Fig. 8.

As depicted in Figs. 7-8, the memory module 100 has a module controller 110 which, like the register 25 in the prior art module, receives the address and command signals from the memory controller and provides registered versions of those signals to two ranks of memory devices 140A-H and 142A-H. Halbert, [0048]-[0049]. Memory module 100, as illustrated by modules 100A-C in Fig. 8, can be attached to memory bus sockets 28A-C. Unlike the prior art module, however, memory module 100 includes interface circuits (shown as interface circuits 125 and 130 in Fig. 7 and data interface circuit 120 in Fig. 4) between memory bus 22, on one side, and corresponding memory devices in ranks 140 and 142, on the other side. The interface circuits are controlled by the module controller 110 through control signals. Halbert, [0048]; Decl., ¶ 73.

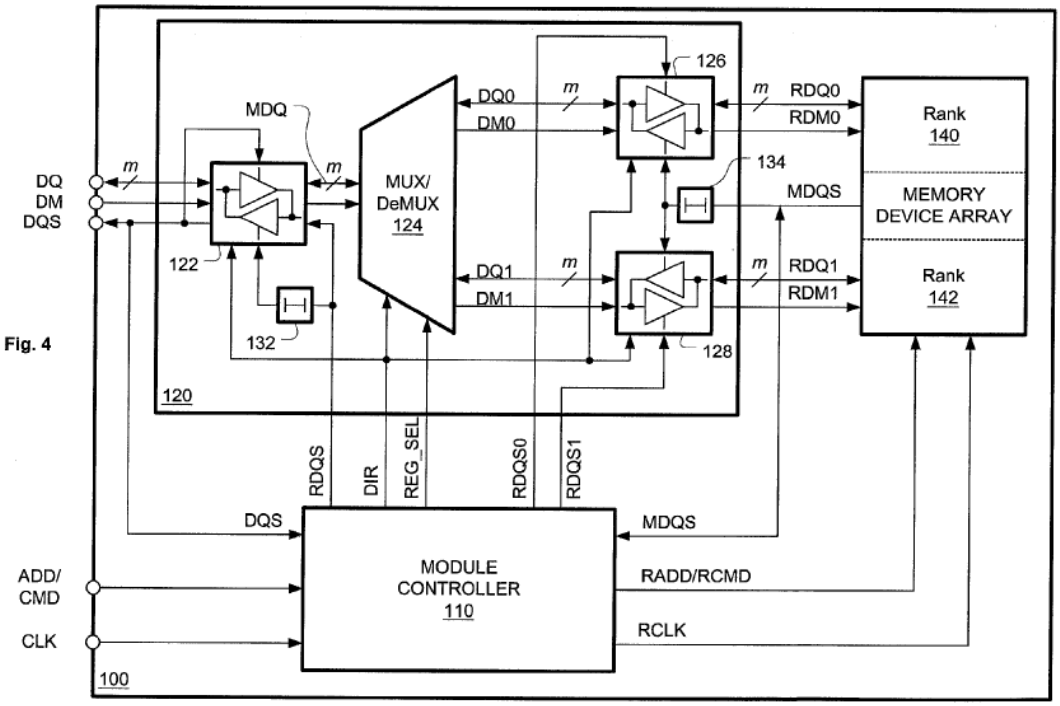


Fig. 4

Halbert, Fig. 4.

Referring to Fig. 4, on the memory bus side (to the left in Fig. 4), the interface circuit 120 has a bi-directional buffer 122 that receives and drives data signals DQ from/to the system memory controller. Halbert, [0031]. The bi-directional buffer 122 can also drive data strobe signals DQS onto the memory bus. *Id*. On the memory rank side (to the right in Fig. 4), the interface circuit 120 has two bi-directional registers 126 and 128 to connect to the memory ranks 140 and 142, respectively. *Id*., [0032]. Signals communicated between buffer 122 and registers 126 and 128 are switched by a multiplexer/demultiplexer 124. Decl., ¶ 74.

The interface circuit 120 is controlled by the module controller 110 using signals. Halbert, [0034]-[0036]. "For instance, direction signal DIR specifies

whether data flow is towards the memory array (TO) or away from the memory array (AWAY)." *Id*., [0034]. "The register select signal REG_SEL, in the AWAY mode, determines whether DQ0 [from Rank 140] or DQ1 [from Rank 142] will be supplied to buffer 122 … [which] drives that data onto the memory data bus." *Id*., [0035]. "In the TO mode, REG_SEL determines which of registers 126 and 128 will receive DQ at each memory bus clock cycle." *Id*., [0036]; Decl., ¶ 75.

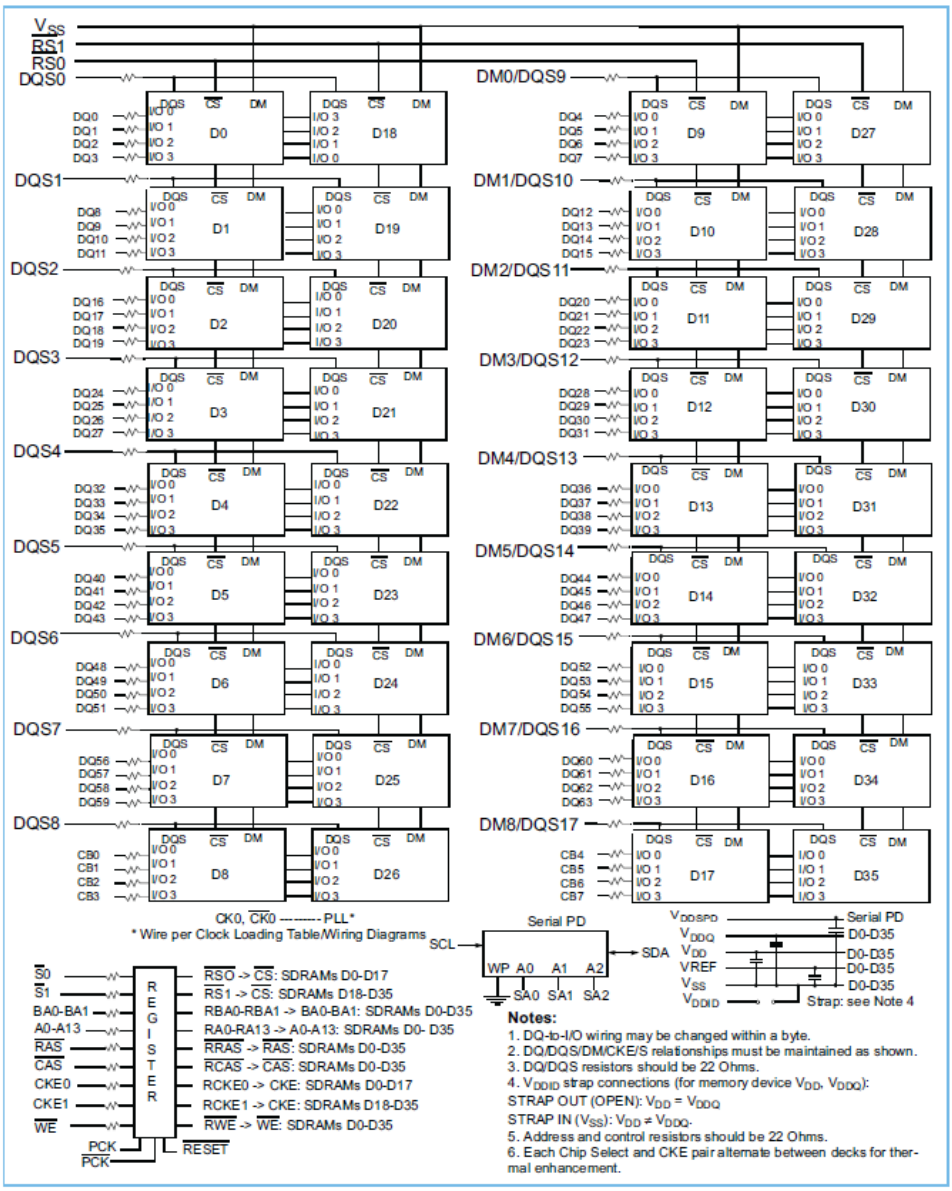
2. Overview of JESD21-C

JESD21-C is an SDRAM Registered DIMM Design Specification. JESD21-C published in January 2002 and qualifies as prior art under pre-AIA 35 U.S.C. §§ 102(a)-(b).

JESD21-C is a specification that "defines the electrical and mechanical requirements for specific types of SDRAM DIMMs that are intended for use as main memory when installed in systems such as servers and workstations." JESD21-C, 5. JESD21-C provides reference design examples to "provide an initial basis for Registered DIMM designs." *Id*.; Decl., ¶ 79.

JESD21-C provides several example architecture block diagrams of DDR SDRAMs. An example architecture block diagram of two physical banks of x4 DDR SDRAMs is shown below.

Block Diagram: Raw Card Version N (Populated as two physical banks of x4 DDR SDRAMs)



JESD21-C, 15. Raw Card Version N shows eighteen 4-bit wide memory devices configured in nine pairs. The D0-D8 and D9-D17 memory devices are selected for data transfers by RS0[bar], and the D18-D26 and D27-D35 memory devices are selected for data transfers by RS1[bar]. Decl., ¶ 81.

B. Ground 1: Halbert in View of JESD21-C Render Claims 15-20 and 22-33 Obvious

1. Claim 15

a. Limitation [15.1]

Halbert discloses Limitation [15.1]. Halbert Fig. 8 depicts "three of the [memory] modules depicted in FIG. 7 arranged in a memory system with a primary memory controller 20 and a multi-drop memory bus 22." Halbert, [0049].

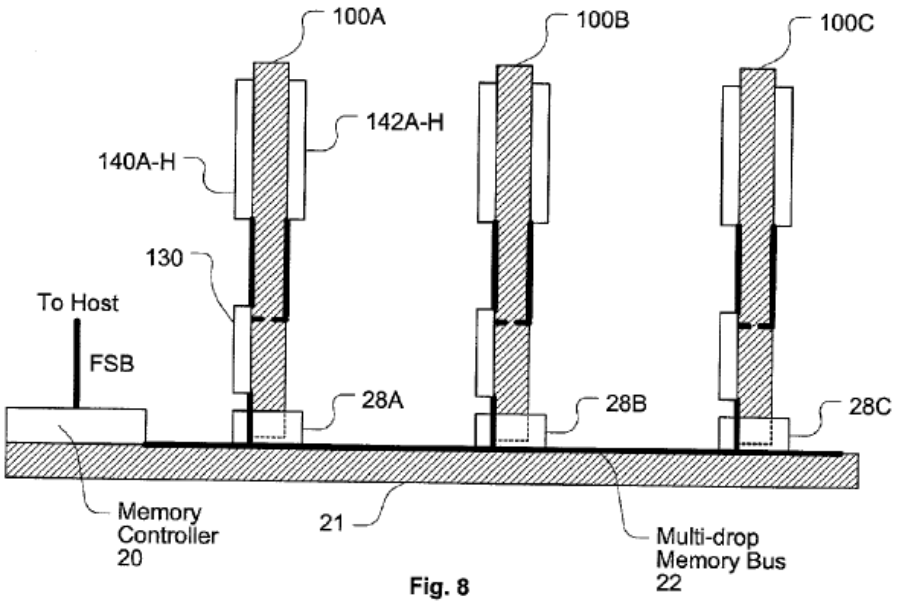


Fig. 8

Id., Fig. 8; Decl., ¶ 233.

Halbert further discloses the components of a memory module, e.g., as depicted in Fig. 4 below.

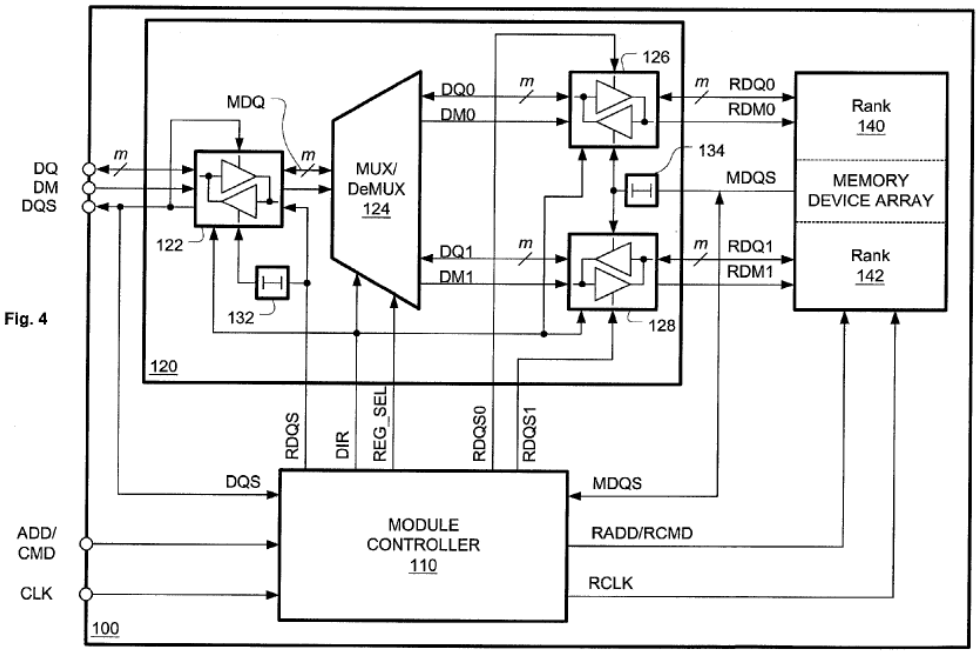


Fig. 4

Halbert, Fig. 4. Memory module 100 has a data interface circuit 120 that "provides for m-bit-wide data transfers between the module and the system memory data bus, and for R×m-bit-wide data transfers between the interface circuit and the memory device array. In FIG. 4, R=2, i.e., the memory device array comprises two memory device ranks 140 and 142." *Id*., [0030]. Data transfers are in response to memory commands received from memory controller 20. "Command signals instruct a memory device as to what type of operation is to be performed, e.g., read, write, refresh …" *Id*., [0005]; Decl., ¶¶ 234-235.

Halbert discloses that a read command causes memory module 100 to output data signals. "In FIG. 4, either data signals DQ0 (from register 126) or data signals DQ1 (from register 128) can be multiplexed to buffer 122 when the module is reading from memory device array 140/142." Halbert, [0033]. In the AWAY (read)

mode, "register data strobe RDQS is functional. When RDQS transitions, buffer 122 latches data from MUX 124 and drives that data onto the memory data bus." *Id*., [0035], Fig. 5; Decl., ¶ 235.

Halbert further discloses that a write command causes memory module 100 to receive data signals. "[W]hen the module is writing to the memory device array, data signals MDQ from buffer 122 can be channeled to either DQ0 or DQ1." Halbert, [0033]. In the TO (write) mode, "[c]ontroller 110 strobes the memory device array, using the memory data strobe MDQS, to signal the array to write data from buses RDQ0 and RDQ1." *Id*., [0036], Fig. 6; Decl., ¶ 236.

b. Limitation [15.2]

Halbert discloses Limitation [15.2]. Memory module 100 is a printed circuit board. Halbert's claim 11 recites "… the module is a dual-inline memory module comprising a printed circuit board capable of connection to the memory data bus via insertion of the circuit board into a card edge connector connected to the memory data bus." Halbert, claim 11. Halbert discloses this in its figures, e.g., in Fig. 8, memory modules 100 in DIMM form factor are plugged into sockets 28A-C of a main board. "Memory controller 20 mounts to motherboard 21 and connects to one end of the leads comprising memory bus 22. Each drop of memory bus 22 connects to an electrical terminator, or socket." *Id*., [0006].

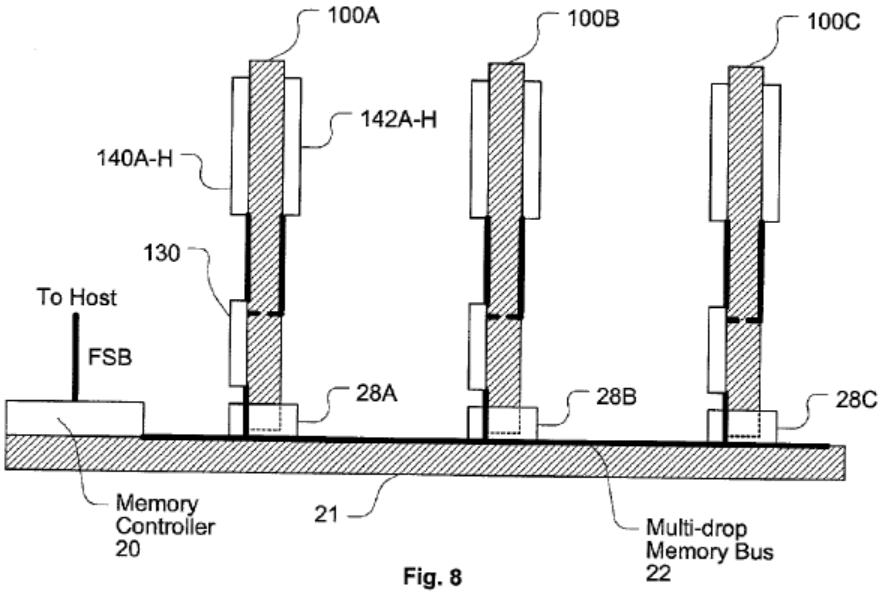


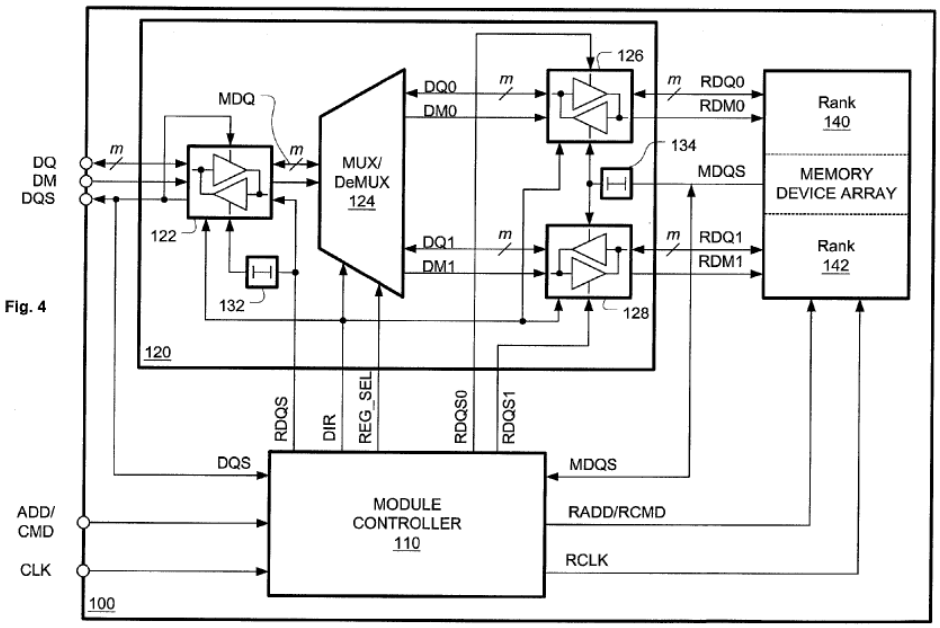
Fig. 8

Id., Fig. 8; *see also id*., [0007]; Decl., ¶¶ 238-240.

c. Limitation [15.3]

Halbert discloses Limitation [15.3]. Halbert discloses module controller 110 as the logic coupled to the printed circuit board, i.e., memory module 100. "Module controller 110 synchronizes the operation of the data port buffer 122, MUX/DeMUX 124, and data registers 126 and 128 via a number of control signals. For instance, direction signal DIR specifies whether data flow is towards the memory array (TO) or away from the memory array (AWAY)." Halbert, [0034]. Data flow away from the memory array means module controller 110 is responding to the read command by providing control signals, i.e., AWAY, to the circuitry, i.e., data interface circuit 120. Decl., ¶ 242. "For instance, DIR can default to TO, and switch to AWAY when the command signals latched into RCMD indicate an impending READ operation." Halbert, [0034]. The logic, module controller 110, can receive a first

set of input address and control signals associated with a first read command and "provide … registered versions of address and command signals, RADD/RCMD." *Id*., [0029]. Specifically, "[a]ddress and command signals ADD/CMD are latched into a register 25 at the edge of one clock cycle, and then redriven onto the module addressing/command bus as register signals RADD/RCMD." *Id*., [0009]. This happens in module controller 110 shown in Fig. 4 below.

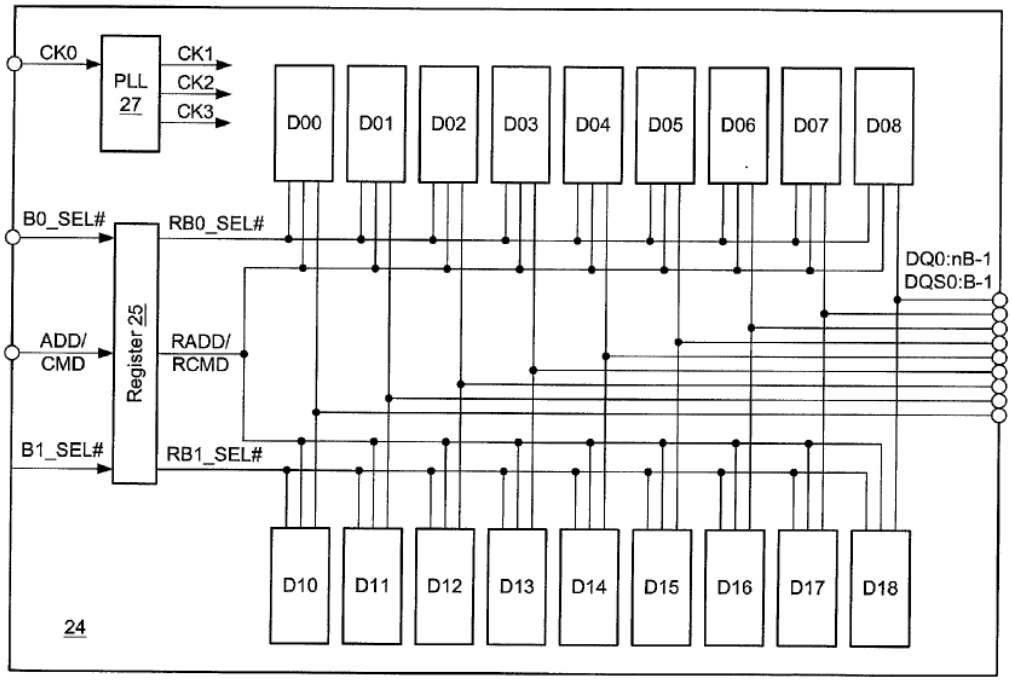


Id., Fig. 4; Decl., ¶ 243. Fig. 4 shows a first set of input address and control signals, i.e., ADD/CMD, which is associated with the read command, input into module controller 110 and a first set of registered address and control signals, i.e., RADD/RCMD, output from the module controller 110. *See also id*., Fig. 5 (showing RCMD and RADD). Decl., ¶ 243.

d. Limitation [15.4]

Halbert discloses Limitation [15.4]. In describing registered DIMM designs, as depicted in Fig. 2 below, Halbert discloses that there are "two bank select signals, B0_SEL# and B1_SEL#, each pass[ing] through register 25 and connect[ing] to a chip select pin on a corresponding one of the banks of memory devices." Halbert, [0009].

Fig. 2
(Prior Art)



Id., Fig. 2. B0_SEL# and B1_SEL# are a first plurality of input chip select signals corresponding to the D00-D08 and D10-D18 memory ranks, respectively, and are part of the first set of input address and control signals for the read operation, i.e., ADD/CMD. Decl., ¶ 244.

Referring to Fig. 4, it would have been obvious to a POSITA to include the first plurality of input chip select signals B0_SEL# and B1_SEL# with the ADD/CMD signals sent by the same memory controller to module controller 110, similar to B0_SEL# and B1_SEL# input to register 25 in Fig. 2, to correspond to memory device ranks 140 and 142, respectively, because Halbert discloses, e.g., "a primary memory controller initiates READ operations [for memory module 100] just like it would for a registered DIMM." Halbert, [0037]. Memory Module 100 is just another design of a registered DIMM, so it would have been obvious to include B0_SEL# and B1_SEL# with the ADD/CMD signals of Fig. 4. Decl., ¶ 245. Module controller 110 in Fig. 4 would have a plurality of chip selects as inputs because there are multiple memory device ranks 140 and 142, and there would be chip selects to select whether data is transferred to/from memory device rank 140 or 142.

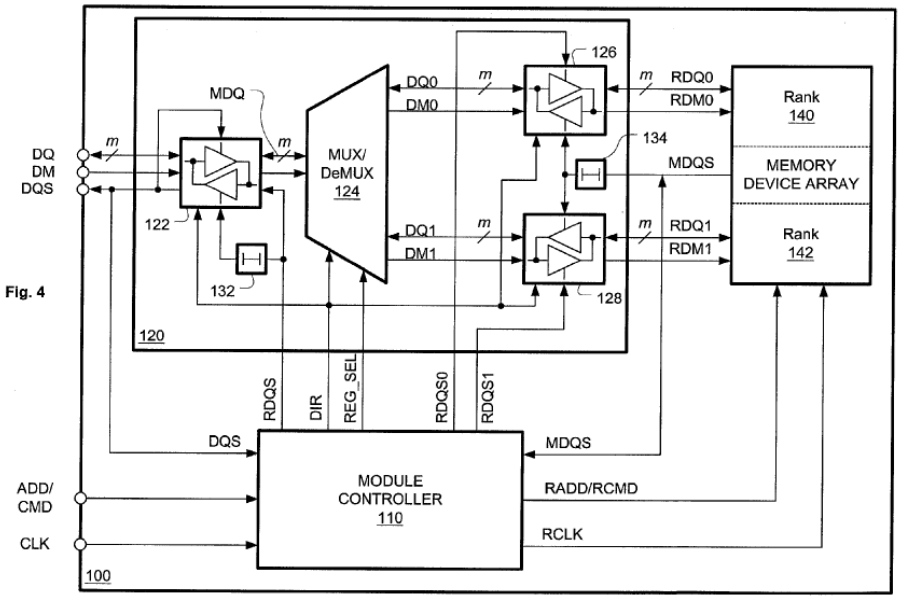
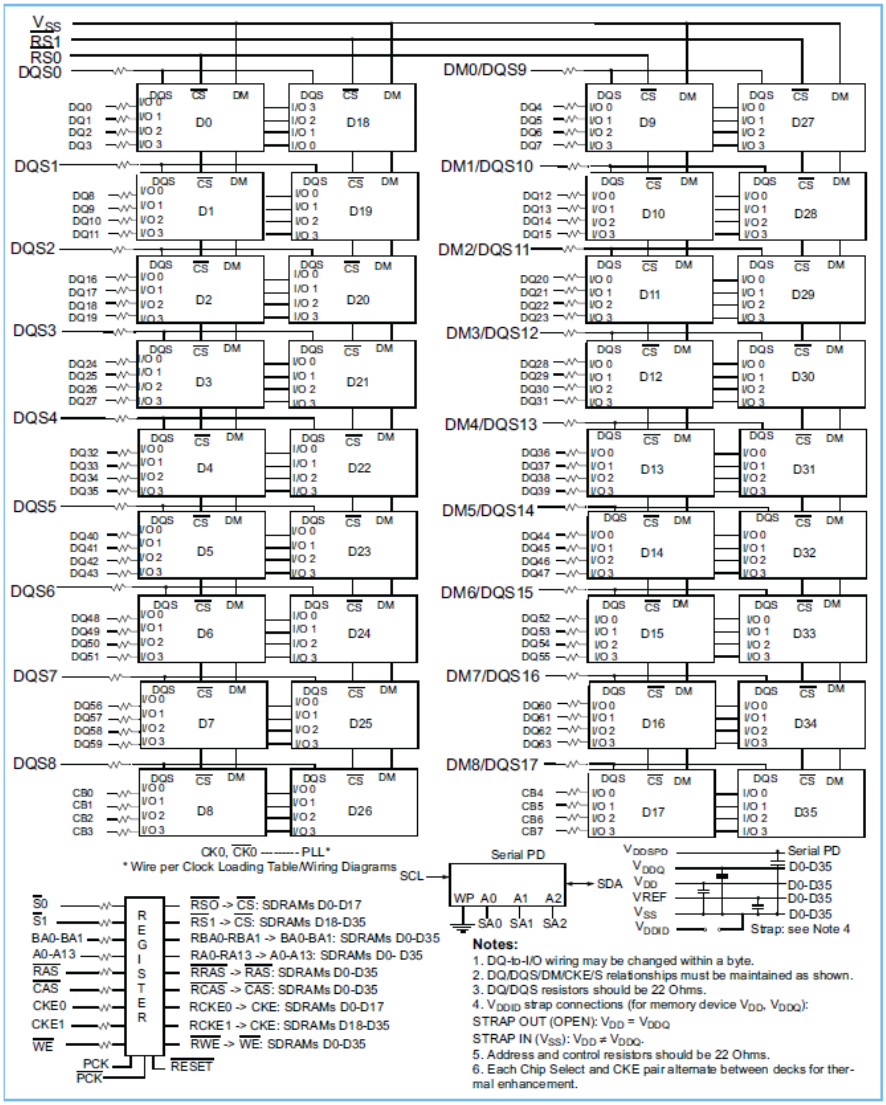


Fig. 4

Halbert, Fig. 4; Decl., ¶ 245.

To the extent Halbert does not teach this limitation, it would have been obvious in view of JESD21-C. JESD21-C discloses a first plurality of input chip select signals S0 and S1 input to the register, as shown in Block Diagram: Raw Card Version N ("Card N") below. Chip select S0 corresponds to the rank that includes the D0-D17 memory devices, and chip select S1 corresponds to the rank that includes the D18-D35 memory devices.

Block Diagram: Raw Card Version N (Populated as two physical banks of x4 DDR SDRAMs)



JESD21-C, 15; Decl., ¶ 246. JESD21-C's Card N discloses a block diagram of two physical banks of x4 DDR SDRAMs, which is what is disclosed in Fig. 4 of Halbert, i.e., memory device ranks 140 and 142. Thus, like Fig. 2 in Halbert, there would be a first plurality of chip selects input to module controller 110 in Fig. 4. *Id*.

Furthermore, a POSITA would have been motivated to combine the teachings of Halbert with JESD21-C because both references are in the same field and directed

toward solving the same problem, i.e., improving the design of memory modules that use SDRAM. Decl., ¶ 247. More specifically, a POSITA would have been motivated to design memory modules and DDR SDRAMs, such as those disclosed in Halbert, to be in compliance with an industry-wide governing standard such as JEDEC. *Id*. A POSITA would have understood that modifying Halbert's memory module 100 shown in Fig. 4 with the teachings of JESD21-C would have been obvious because Halbert is directed to "memory module configurations and access methods … [that] can improve on the dual-bank registered DIMM in several respects" (Halbert, [0024]), and JESD21-C is a specification that "defines the electrical and mechanical requirements for … 64/72 bit-wide, Registered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR SDRAM DIMMs)" (JESD21-C, 5). Decl., ¶ 247. Thus, both references are directed to achieving the same goal, and a POSITA would have been motivated to incorporate any additional standardized DDR SDRAM DIMMs design requirements into Halbert's memory module 100. *Id*.

Moreover, JESD21-C is a specification for specifying the architecture for different DDR SDRAM DIMMs.

Product Family Attributes

DIMM organization	x72 ECC, x64
DIMM dimensions (nominal)	5.25" x 1.2"/1.7"
Pin count	184
SDRAMs supported	64Mb, 128Mb, 256Mb, 512Mb, 1Gb
Capacity	64MB, 128MB, 256MB, 512MB, 1GB, 2GB, 4GB
Serial PD	Consistent with JC 42.5 Rev 0
Voltage options	2.5 volt (V_{DD}/V_{DDQ})
Interface	SSTL_2

JESD21-C, 5; Decl., ¶ 248. This is the exact type of memory device that is disclosed in Halbert. "Some possible device types include dynamic random access memory (DRAM) devices, synchronous DRAM (SDRAM) devices including double-data-rate (DDR) SDRAM devices, quad-data-rate (QDR) SDRAM devices, Rambus™ DRAM devices (with an appropriate controller), static RAM and flash memory devices." Halbert, [0061]; Decl., ¶ 248. And the basic architecture of memory module 100 of Halbert is the same as some of the memory architectures described in JESD21-C. *See, e.g.*, Halbert, Fig. 4 (showing two memory ranks, 140 and 142, in the memory device array) and JESD21-C, 15 (showing Card N with two memory ranks, D0-D17 and D18-D35); Decl., ¶ 248.

Further, both Halbert's memory module 100 and the SDRAM DDR DIMM designs disclosed in JESD21-C implement similar prior art functional designs for memory devices. Decl., ¶ 249. For example, memory module 100's data interface circuit 120 in Halbert and the SDRAM DDR DIMM designs disclosed in JESD21-C both include registers to add a predetermined time delay of one clock cycle for each registered data transfer through the memory module's circuitry. *See, e.g.*,

Halbert, Fig. 5 (showing a one clock cycle delay between the time when register 126 latches a first piece of data (DO_a1) onto bus DQ0 and when it latches the next piece of data (DO_b1) onto bus DQ0) and JESD21-C, 68 ("In a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM CAS latency)."); Decl., ¶ 249. And both Halbert and JESD21-C disclose the use of chip selects to select different memory ranks. *See, e.g.*, Halbert, [0009] ("Note that two bank select signals, B0_SEL# and B1_SEL#, each pass through register 25 and connect to a chip select pin on a corresponding one of the banks of memory devices.") and JESD21-C, 15 (showing chip select signal S0 corresponding to the D0-D17 memory devices and S1 corresponding to the D18-D35 memory devices); Decl., ¶ 249.

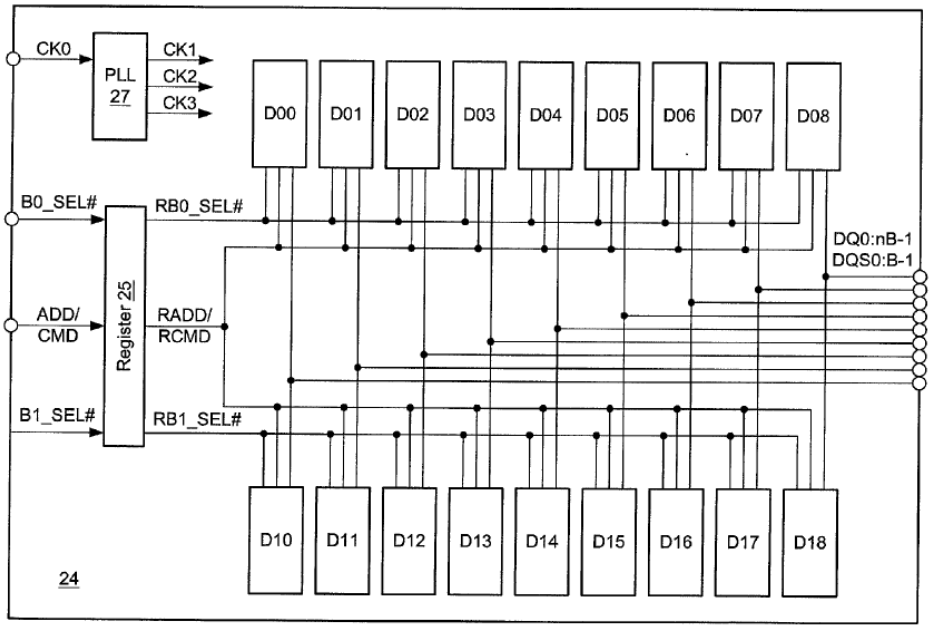
Applying the teachings of JESD21-C to Halbert would not have been beyond the skill of a POSITA and would follow the typical course of technological progression. Decl., ¶ 250. A POSITA would have understood that the number and configuration of ranks and memory integrated circuits in a memory module, as well as the use of chip selects for selecting memory ranks and registers for data transfers, are design choices. *Id*. Accordingly, modifying Halbert's memory module 100 to incorporate one of the many different DDR SDRAM architectures and features disclosed in the contemporaneous JESD21-C would have been obvious. *Id*. Indeed, Halbert contemplates different DDR SDRAM architectures. "The data lines DQ of

the memory device banks each connect to the memory bus of the host system. A total of nB DQ lines carry data signals, where B is the number of devices in one bank (e.g., eight or nine), and n is the data width of each device (e.g., four, eight, or sixteen bits)." Halbert, [0009]. Such a modification would also have been obvious because it was one of a finite number of solutions, not beyond the skill of an ordinary artisan to implement, and would have yielded predictable results. Decl., ¶ 250. Thus, a POSITA would have been motivated to incorporate the teachings of JESD21-C into the memory system of Halbert. *Id*.

e. Limitation [15.5]

Halbert discloses Limitation [15.5]. Halbert discloses that the "two bank select signals, B0_SEL# and B1_SEL#, each pass through register 25 and connect to a chip select pin on a corresponding one of the banks of memory devices." Halbert, [0009]. Thus, along with the first set of registered address and control signals, i.e., RADD/RCMD, Halbert discloses RB0_SEL# and RB1_SEL# as a first plurality of registered chip select signals that correspond to the first plurality of input chip select signals, i.e., B0_SEL# and B1_SEL#, respectively, as shown in Fig. 2.

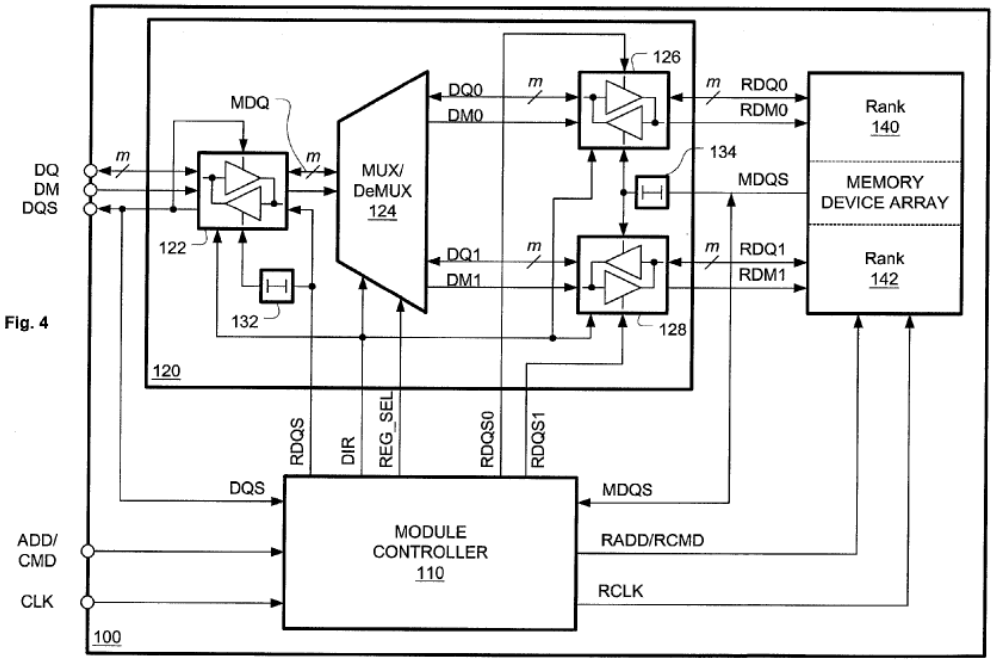
Fig. 2
(Prior Art)



Id., Fig. 2; Decl., ¶ 251.

Referring to Fig. 4, it would have been obvious to a POSITA to include the first plurality of registered chip select signals RB0_SEL# and RB1_SEL# that correspond to the first plurality of input chip select signals B0_SEL# and B1_SEL#, respectively, with the RADD/RCMD signals output by module controller 110, similar to RB0_SEL# and RB1_SEL# output from register 25 in Fig. 2, because Halbert discloses, e.g., "a primary memory controller initiates READ operations [for memory module 100] just like it would for a registered DIMM." Halbert, [0037]. Memory Module 100 is just another design of a registered DIMM, so it would have been obvious to include RB0_SEL# and RB1_SEL# with the RADD/RCMD signals of Fig. 4. Decl., ¶ 252. Module controller 110 in Fig. 4 would have a plurality of registered chip selects as outputs because there are multiple memory device ranks

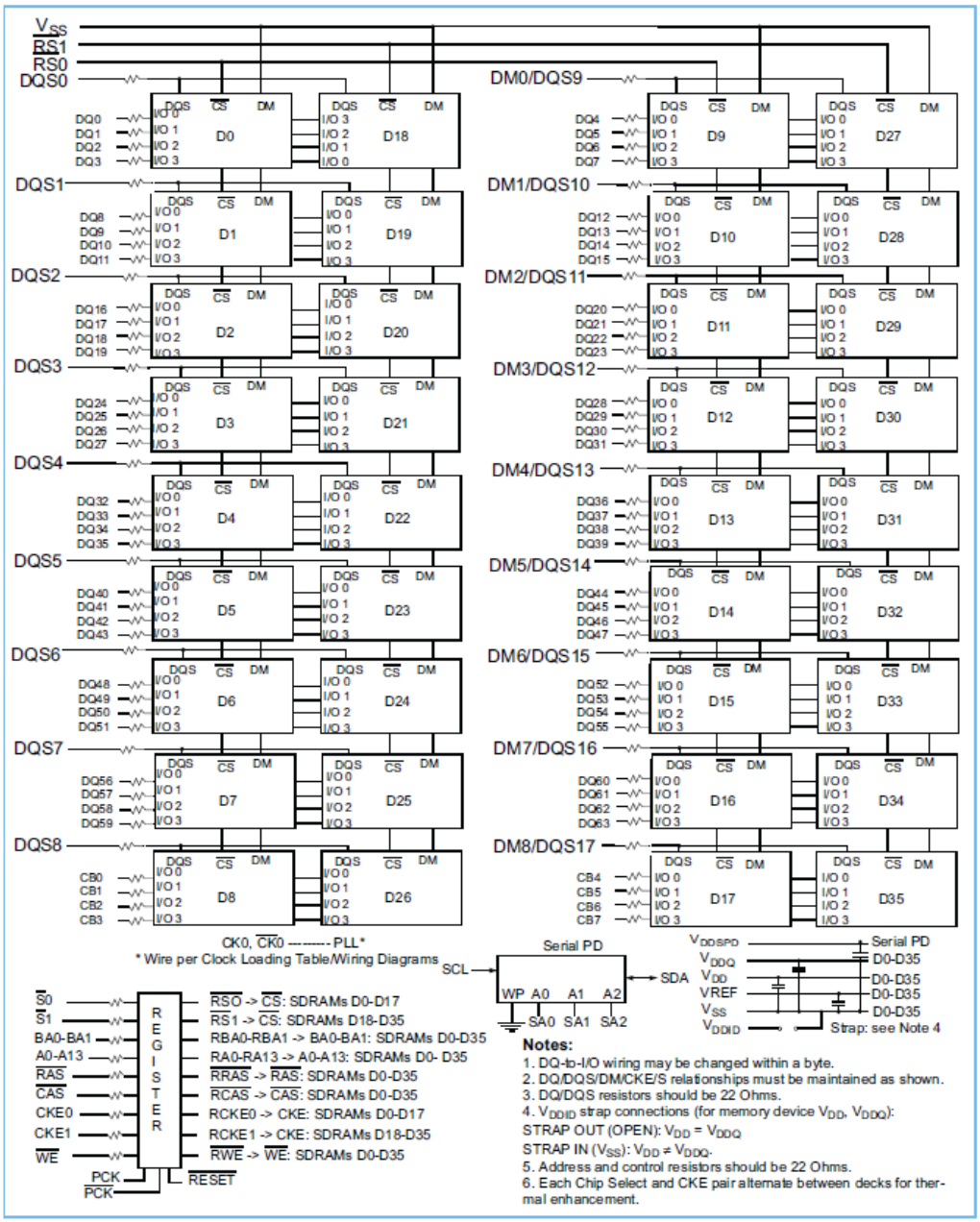
140 and 142, and there would be registered chip selects to select whether data is transferred to/from memory device rank 140 or 142.



Halbert, Fig. 4; Decl., ¶ 252.

To the extent Halbert does not teach this limitation, it would have been obvious in view of JESD21-C. JESD21-C discloses a first plurality of registered chip select signals RS0 and RS1 output from the register, as shown in Card N below. RS0 and RS1 correspond to the first plurality of input chip select signals S0 and S1 and are shown as input to each bank of memory ranks. Registered chip select RS0 corresponds to the D0-D17 memory ranks, and registered chip select RS1 corresponds to the D18-D35 memory ranks.

Block Diagram: Raw Card Version N (Populated as two physical banks of x4 DDR SDRAMs)



JESD21-C, 15; Decl., ¶ 253. JESD21-C's Card N discloses a block diagram of two physical banks of x4 DDR SDRAMs, which is what is disclosed in Fig. 4 of Halbert, i.e., memory device ranks 140 and 142. Thus, like Fig. 2 in Halbert, there would a

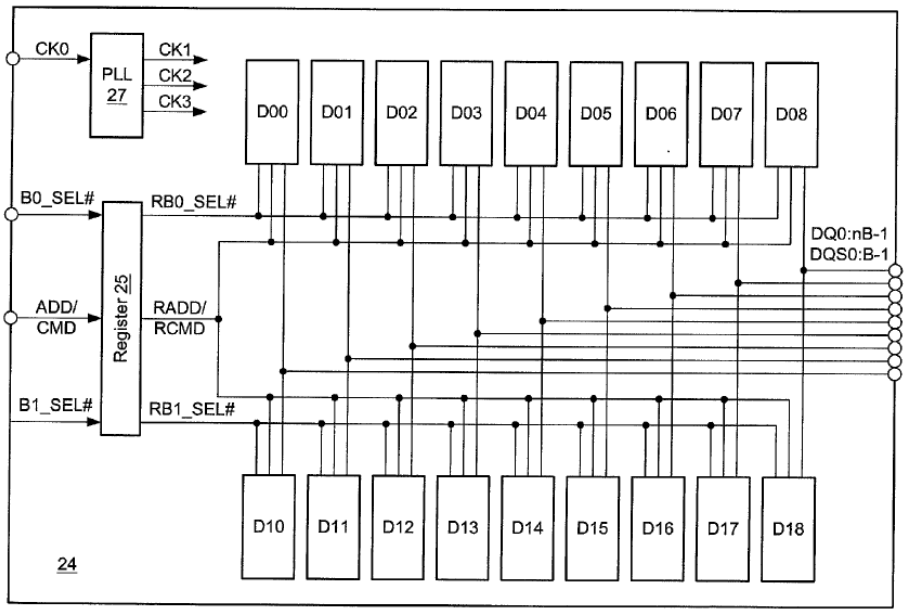
first plurality of registered chip selects output from module controller 110 in Fig. 4 that correspond to the first plurality of input chip select signals. Decl., ¶ 253.

A POSITA would have been motivated to combine the teachings of JESD21-C with Halbert for at least the reasons specified above. *See* §V.B.1.d; Decl., ¶ 254.

f. Limitation [15.6]

Halbert discloses Limitation [15.6]. As discussed above, Halbert discloses a first plurality of registered chip select signals RB0_SEL# and RB1_SEL#. Referring to Fig. 2 below, RB0_SEL# has an active signal value when selecting the D00-D08 memory ranks for data transfers. When RB0_SEL# has an active signal value, RB1_SEL# has a non-active signal value because the D10-D18 memory ranks are not selected for data transfers.

Fig. 2
(Prior Art)



Halbert, Fig. 2; Decl., ¶ 255.

RB0_SEL# having an active signal value while RB1_SEL# has a non-active signal value is reflected in Fig. 3 below.

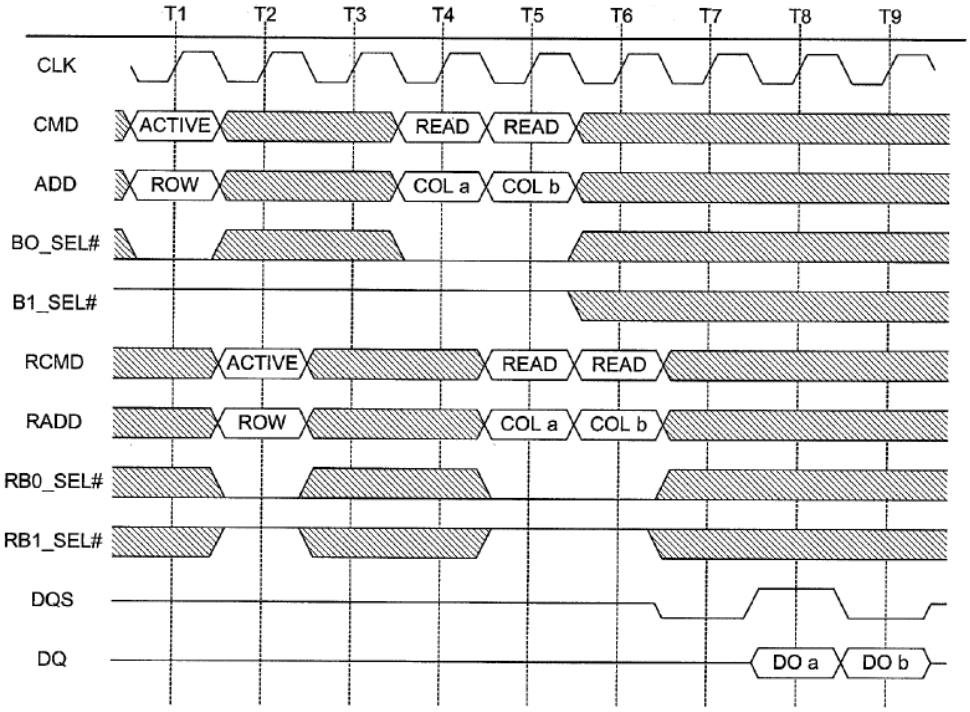


Fig. 3
(Prior Art)

Halbert, Fig. 3. As shown in Fig. 3, RB0_SEL# is low to indicate that it has an active signal value at all times the registered address and control signals are active, while RB1_SEL# is high to indicate that it has a non-active signal value during those times. Decl., ¶ 256.

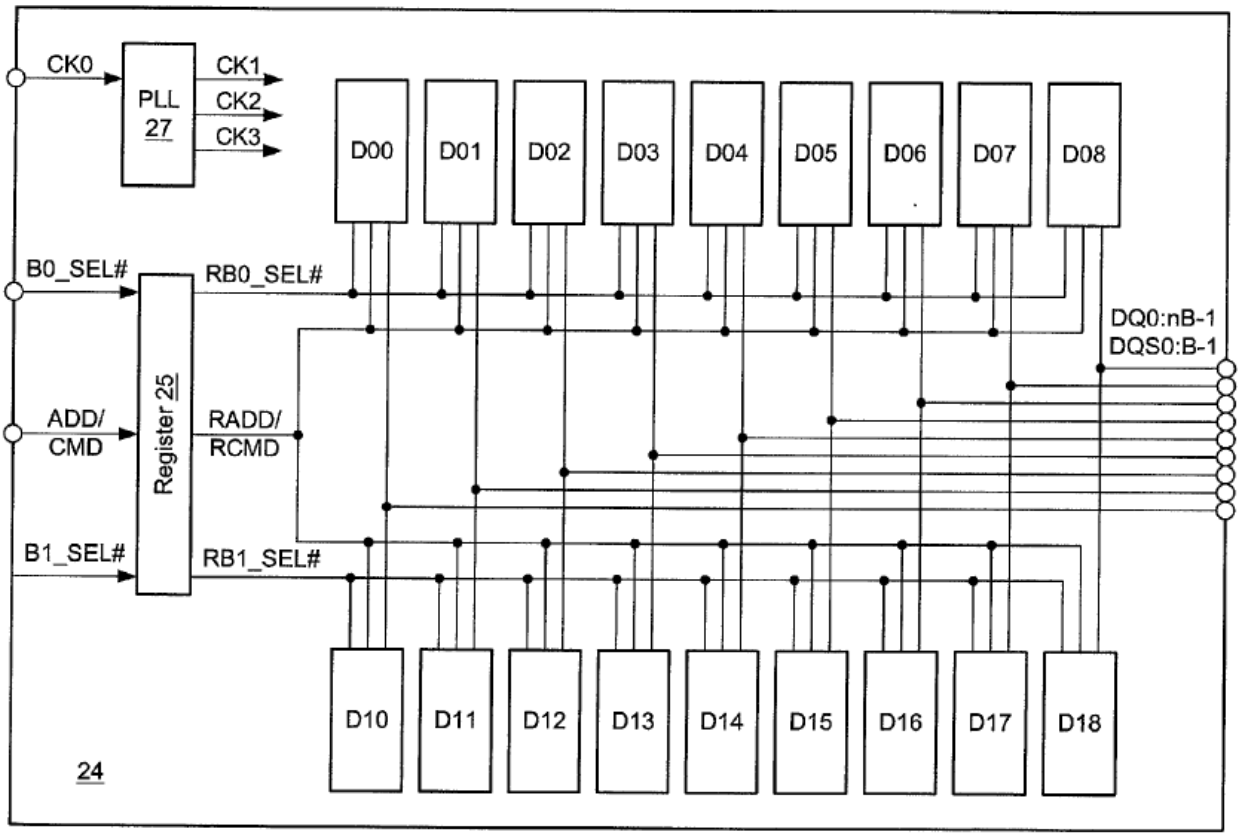
g. Limitation [15.7]

Halbert discloses Limitation [15.7]. Halbert's "FIG. 4 illustrates a block diagram for one embodiment of a memory module 100 [that includes] a memory device array 140/142." Halbert, [0027]-[0028]. Memory device array 140/142 are memory integrated circuits mounted on the printed circuit board, i.e., memory

module 100, and arranged in a plurality of N-bit wide ranks. *See id*., [0030] ("In FIG. 4, R=2, i.e., the memory device array comprises two memory device ranks 140 and 142, each capable of performing m-bit-wide data transfers."); Decl., ¶ 258.

Halbert further discloses that the plurality of N-bit wide ranks is configured to receive the first plurality of registered chip select signals. The "two bank select signals, B0_SEL# and B1_SEL#, each pass through register 25 and connect to a chip select pin on a corresponding one of the banks of memory devices." Halbert, [0009]. After B0_SEL# and B1_SEL# pass through register 25, RB0_SEL# is received by the D00-D08 memory rank, and RB1_SEL# is received by the D10-D18 memory rank, as shown in Fig. 2 below.

Fig. 2
(Prior Art)



Id., Fig. 2. Referring to Fig. 4, a POSITA would understand that, similar to register 25 in Fig. 2, module controller 110 can output RB0_SEL# to be received by memory rank 140 and RB1_SEL# to be received by memory rank 142. Decl., ¶ 259.

h. Limitation [15.8]

Halbert discloses Limitation [15.8]. As discussed above for Limitation [15.6], if RB0_SEL# has the active signal value and RB1_SEL# has the non-active signal value, then one of two memory ranks is active while the other memory rank is non-

active, e.g., memory device rank 140 is active while memory device rank 142 is non-active.

Halbert discloses that memory device rank 140 can be configured to output the first burst of N-bit wide data signals and a first burst of data strobes associated with the read command. "In FIG. 4, either data signals DQ0 (from register 126) or data signals DQ1 (from register 128) can be multiplexed to buffer 122 when the module is reading from memory device array 140/142." Halbert, [0033]. Data is output from memory device array 140 on bus RDQ0. *See id*., [0038] ("Controller 110 asserts DIR (where asserted equals AWAY) sometime after passing the first READ command to device array 140/142. This assertion time can vary, but preferably occurs prior to when device array 140/142 is expected to begin driving buses RDQ0 and RDQ1."); Decl., ¶ 261.

If memory device array 140 is the active rank, memory device array 140 outputs the first burst of N-bit wide data signals, which occurs in response to the read command. "In the ACTIVE state, controller 110 scans the command bus for READ or WRITE commands … At T4, a READ command (to COL a) is clocked in, causing the controller to enter a READ state." Halbert, [0037]. Data signal DQ0 is output to the memory data bus. "The register select signal REG_SEL, in the AWAY mode, determines whether DQ 0 or DQ1 will be supplied to buffer 122. Data is serialized from the data registers onto the memory data bus by reading 2m

bits into the data registers during one memory device read cycle, and then driving these bits, m at a time, through MUX 124." *Id*., [0035], Fig. 5. Memory device array 140 also outputs a first burst of data strobes, i.e., memory data strobe MDQS, as part of the read operation. "MDQS will comprise multiple strobes, each device in device array 140/142 supplying at least one strobe synchronized to its data signals." *Id*., [0038]; Decl., ¶ 262. The receipt and output of data strobes MDQS by each of the memory devices meets Netlist's proposed alternative construction of "burst of data strobes" because the data strobe signals MDQS have "successive rising and falling edges, each edge being associated with a data bit." Decl., ¶ 262 (Figs. 5 and 6 depict data bits associated with the rising and falling edges of MDQS).

i. Limitation [15.9]

Halbert discloses Limitation [15.9]. Fig. 4 of Halbert below discloses the circuitry (data interface circuit 120), between data and strobe signal lines in the N-bit wide memory bus, i.e., shown on the left side with m-bit wide DQ and DQS going to and from memory module 100, and the corresponding data and strobe pins of memory devices in each of the plurality of N-bit wide ranks, i.e., RDQ0, RDQ1, and MDQS of memory device array 140/142.

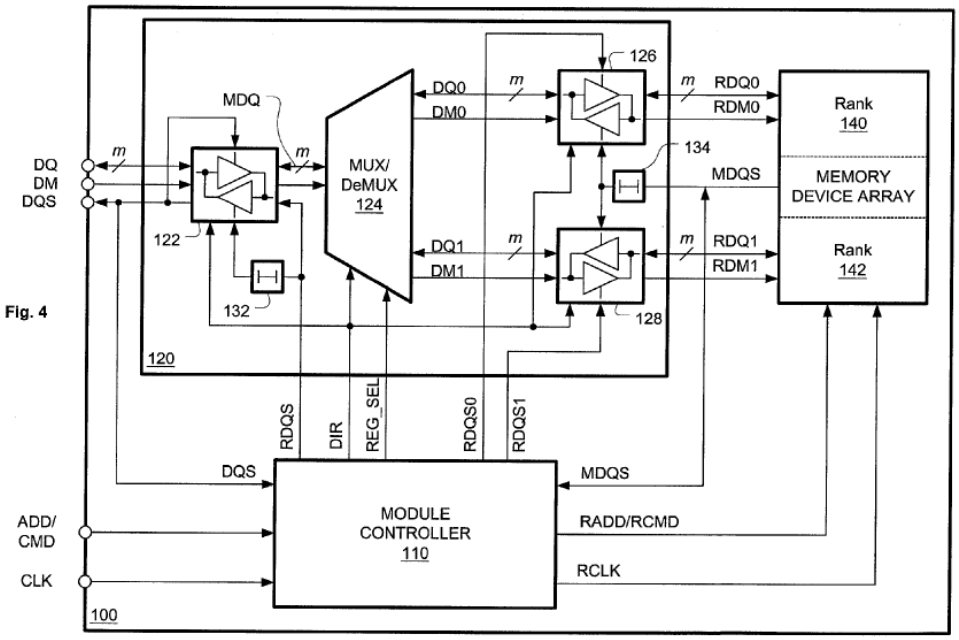


Fig. 4

Halbert, Fig. 4; Decl., ¶ 264.

Halbert discloses that the circuitry, i.e., data interface circuit 120, "provides for m-bit-wide data transfers between the module and the system memory data bus, and for R×m-bit-wide data transfers between the interface circuit and the memory device array. In Fig. 4, R=2, i.e., the memory device array comprises two memory device ranks 140 and 142, each capable of performing m-bit-wide data transfers." Halbert, [0030]; Decl., ¶ 265.

j. Limitation [15.10]

Halbert discloses Limitation [15.10]. Halbert discloses module controller 110 as the logic coupled to the circuitry (data interface circuit 120). "Module controller 110 synchronizes the operation of the data port buffer 122, MUX/DeMUX 124, and data registers 126 and 128 via a number of control signals. For instance, direction

signal DIR specifies whether data flow is towards the memory array (TO) or away from the memory array (AWAY)." Halbert, [0034]. When data flow is away from the memory array, module controller 110 is responding to the first read command by outputting first control signals, i.e., AWAY, to the circuitry, i.e., data interface circuit 120. Decl., ¶ 267.

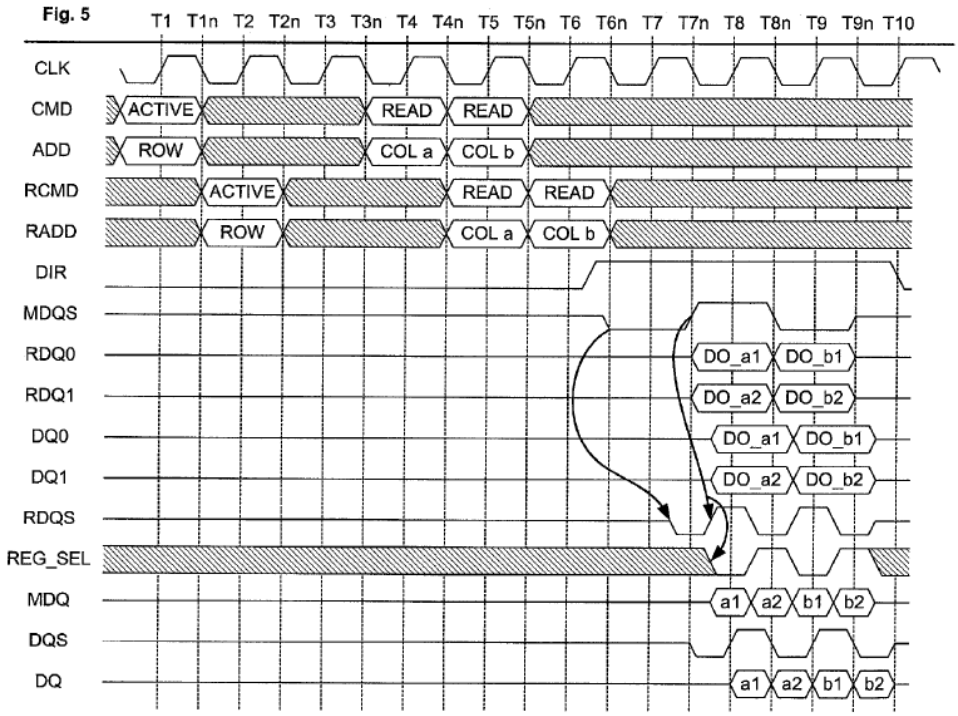
k. Limitation [15.11]

Halbert discloses Limitation [15.11]. Halbert discloses that in response to the first control signals, i.e., in the AWAY mode, data interface circuit 120 enables data transfers from memory device rank 140 through data interface circuit 120 to buffer 122 toward the system memory data bus. "The register select signal REG_SEL, in the AWAY mode, determines whether DQ 0 or DQ1 will be supplied to buffer 122. Data is serialized from the data registers onto the memory data bus by reading 2m bits into the data registers during one memory device read cycle, and then driving these bits, m at a time, through MUX 124." Halbert, [0035]; Decl., ¶ 268.

Halbert further discloses that the respective N-bit wide data signals of the first burst of N-bit wide data signals and respective data strobes of the first burst of data strobes (*see* Limitation [15.8] above) are transferred through the circuitry *in accordance with an overall CAS latency of memory module* 100. "The module controller 110 synchronizes the operation of module 100 with the attached memory system. Like the address/command registers and PLL of a registered DIMM,

controller 110 can provide clock adjustment to an input CLK signal … In addition, module controller 110 provides timing and synchronization signals to data interface circuit 120." Halbert, [0029]. A POSITA would have understood that module controller 110 provides all the necessary signals to synchronize the operation of memory module 100, including in accordance with the overall CAS latency of memory module 100. Decl., ¶ 269. In other words, a POSITA would have understood that because the data transfers occur within a timespan that would be considered the overall CAS latency of the memory module, the data transfers must be transferred in accordance with the overall CAS latency of the memory module. *Id*.

Fig. 5 below shows a timing diagram for two consecutive read operations for the memory module of FIG. 4. The READ command for COL a is clocked in at T4 and data a1 and a2 are available on DQ at T8 and T8n, respectively. Thus, Fig. 5 shows that the N-bit wide data signals of the first burst of N-bit wide data signals and respective data strobes of the first burst of data strobes (which happen at T7n) are transferred through data interface circuit 120 in accordance with an overall CAS latency of memory module 100, i.e., T4 to T8.



Halbert, Fig. 5; Decl., ¶ 270. This meets both sides' proposed construction of "overall CAS latency of the memory module" because T4 to T8 is the "the delay between: (1) the time when a command is executed/sampled on the memory module [the READ command for COL a clocked in at T4], and (2) a time when the first piece of data is available at the output/data pins of the memory module [data a1 available on DQ at T8]." Decl., ¶ 270.

l. Limitation [15.12]

Halbert discloses Limitation [15.12]. As depicted in Fig. 4 below, Halbert discloses registers 126, 128, and 122 for providing registered data transfers through data interface circuit 120. Register 126 provides the registered data transfers between the first rank, i.e., memory device rank 140, and the memory bus 22.

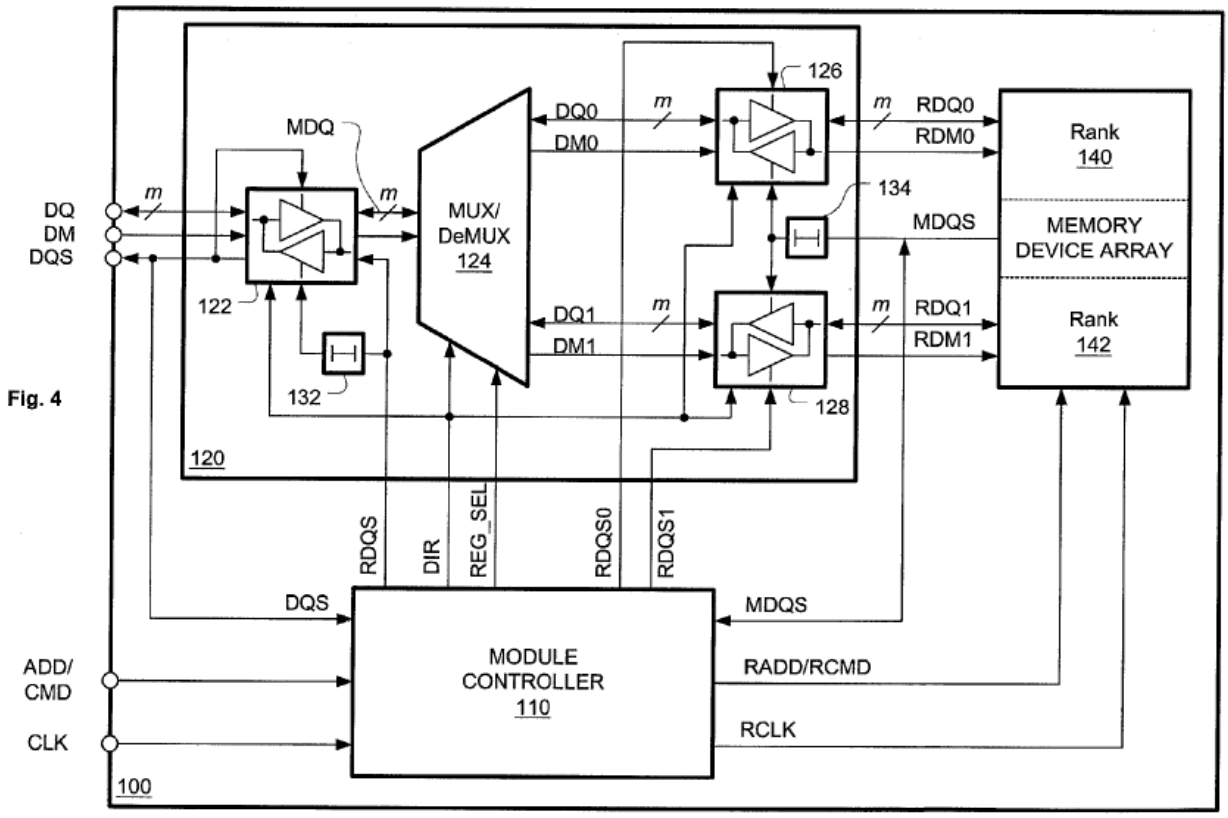
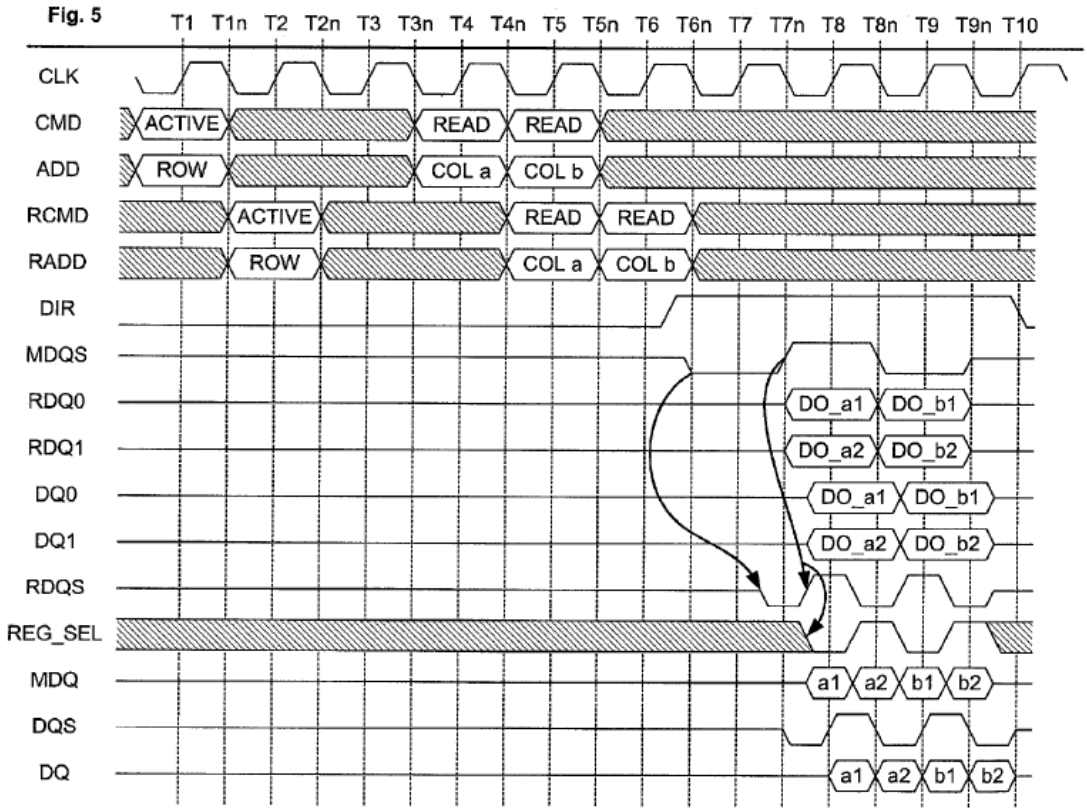


Fig. 4

Halbert, Fig. 4; Decl., ¶ 272. "In FIG. 4, [] data signals DQ0 (from register 126) … can be multiplexed to buffer 122 when the module is reading from memory device array 140[]." Halbert, [0033].

Referring again to Fig. 5 below, data interface circuit 120 is configured to add a predetermined amount of time delay for each registered data transfer through the circuitry, i.e., registers 126 and 128 add a predetermined time delay of one clock cycle for each registered data transfer through circuit 120.



Halbert, Fig. 5; Decl., ¶ 273. Data transfers through the memory module begin with the READ command of COL a clocked in at T4 and of COL b clocked in at T5, respectively. Registers 126 and 128 of the data interface circuit 120 each add a one clock cycle delay to data transfers through circuit 120, as shown, for example, by the one clock cycle delay between the time when register 126 latches a first piece of data (DO_a1) onto bus DQ0 (from bus RDQ0) and the time when register 126 latches the next piece of data (DO_b1) onto bus DQ0 (from bus RDQ0). As a result, the overall CAS latency of memory module 100, e.g., from T4 to T8, is greater than the actual operational CAS latency of each of the memory devices, which is from T5 to T7n (where the data exits the memory device array 140 on RDQ0). Decl., ¶ 273.

A POSITA would understand that "[i]n a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM CAS latency." JESD21-C, 68; Decl., ¶ 274. This meets both sides' proposed construction of "actual operational CAS latency of each of the memory devices" because T4 to T8 is greater than "the delay between: (1) the time when a command is executed by each of the plurality of memory devices [the registered READ command for COL a clocked in at T5], and (2) a time when the first piece of data is available at the output/data pins of each of the plurality of memory devices [where the data exits the memory device array on RDQ0 at T7n]." Decl., ¶ 273.

2. Claim 16

a. Limitation [16.1]

Claim 16 depends on claim 15. The '314 patent states "[a]s used herein, the term 'load' is a broad term which includes, without limitation, electrical load, such as capacitive load, inductive load, or impedance load." Ex. 1001, 6:1-3.

Halbert discloses Limitation [16.1]. Halbert discloses that "[t]he exemplary embodiments also allow the memory devices to be isolated from the full capacitive loading effects of the system memory data bus." Halbert, [0024]. Halbert further discloses that "[t]wo bi-directional data registers 126 and 128 connect, respectively, to memory device array ranks 140 and 142. Each data register can receive an m-bit-

wide word from its corresponding memory device rank, or drive an m-bit-wide word to that rank, over a dedicated point-to-point module data bus." *Id*., [0032]. A POSITA would have understood that each of memory devices, i.e., each of memory device ranks 140 and 142, has a corresponding load, i.e., the capacitive loading of RDQ0 and RDQ1 transfers to and from registers 126 and 128, respectively. Decl., ¶¶ 277-278. "[T]he number of device inputs also determine the capacitance that a memory device (or the controller) sees when it drives the bus." Halbert, [0025]. Thus, the m RDQ lines each has its own capacitive loading associated with it. Decl., ¶ 278.

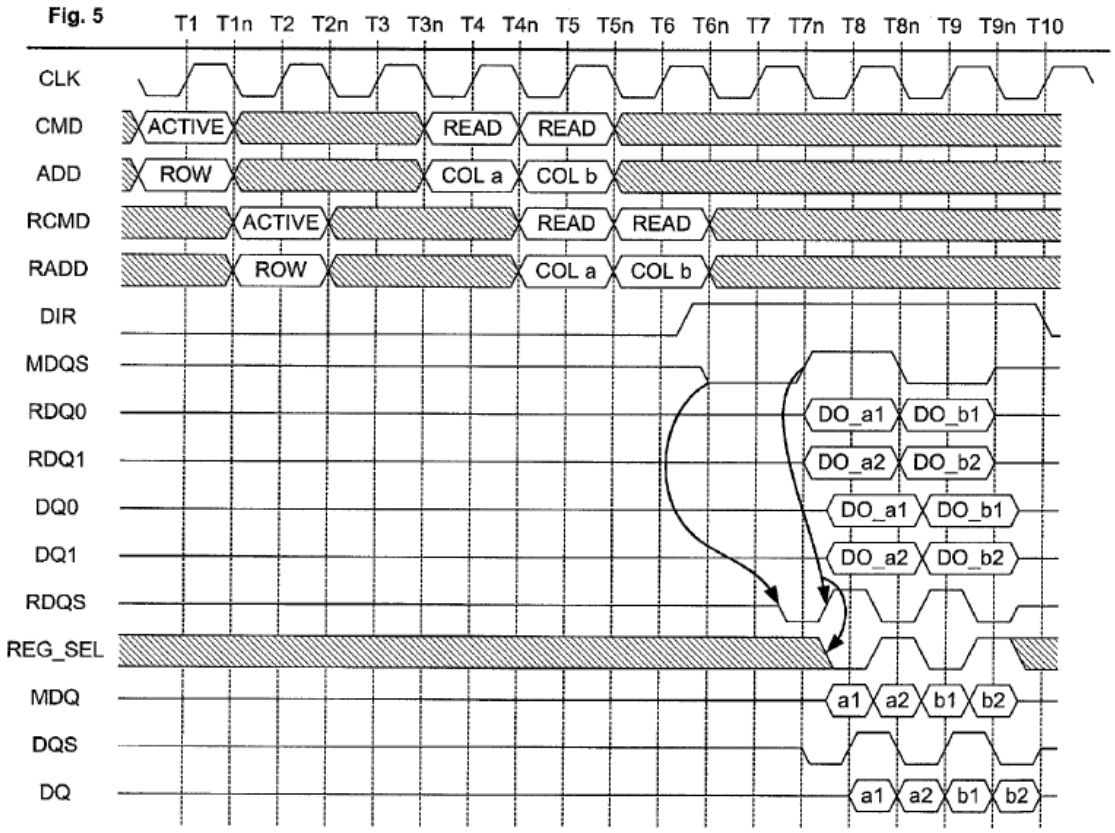
b. Limitation [16.2]

Halbert discloses Limitation [16.2]. Halbert discloses that "[t]he memory systems and modules described herein generally improve upon the multi-drop memory bus architecture by isolating the memory devices on each module from the bus." Halbert, [0026]. Halbert also discloses that "[t]he exemplary embodiments also allow the memory devices to be isolated from the full capacitive loading effects of the system memory data bus." *Id*., [0024]. As depicted in Fig. 4, the circuitry of data interface circuit 120, e.g., multiplexer/demultiplexer (MUX/DeMUX) 124, bi-directional buffer 122, and bi-directional data registers 126 and 128, isolates the loads of the memory devices, i.e., the capacitive loading of RDQ0 and RDQ1, from the memory bus 22 (to the left of Fig. 4), i.e., the input/output on DQ. Decl., ¶ 279.

3. Claim 17

a. Limitation [17.1]

Claim 17 depends on claim 15. Halbert discloses Limitation [17.1]. Fig. 5 of Halbert, shown below, is the timing diagram for two consecutive read operations for memory module 100.

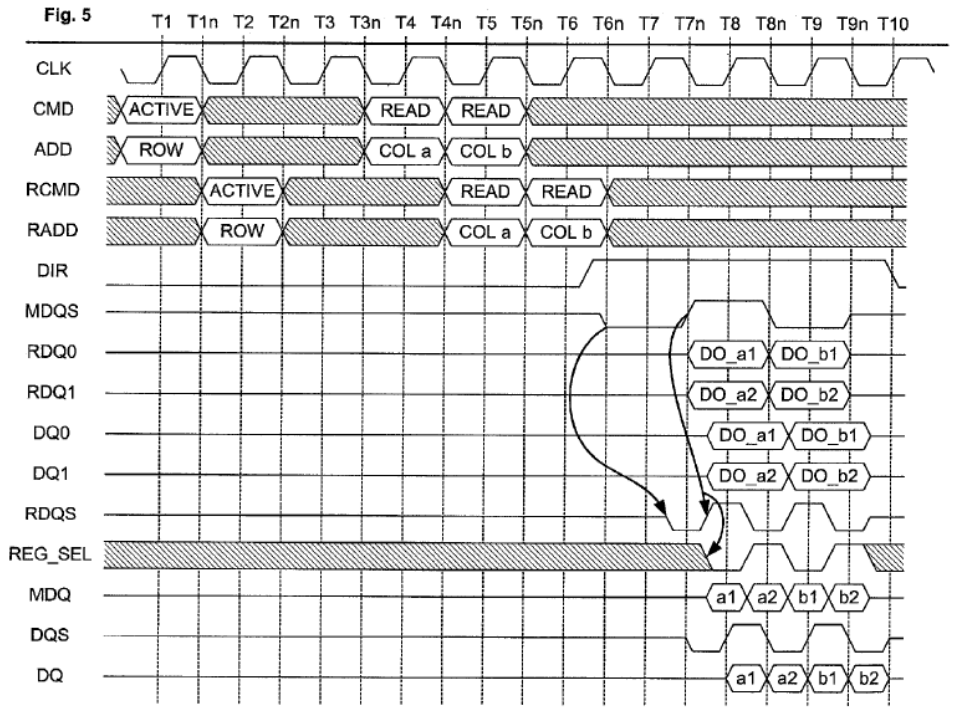


Halbert, Fig. 5. Data transfers of data a and b through the memory module begin with the READ command of COL a clocked in at T4 and of COL b clocked in at T5, respectively. At T7n, Fig. 5 shows that a set of consecutive data bits DO_a1 and DO_b1 for data a and b begins transmission to the memory bus. Accordingly, Fig. 5 discloses and/or renders obvious that the first burst of N-bit wide data signals

includes a set of consecutively transmitted data bits, e.g., DO_a1 transmitted starting at T7n followed immediately on the next clock cycle by DO_b1 transmitted starting at T8n, for each data signal line in the memory bus, e.g., data signal line RDQ0 associated with data signal line DQ in the memory bus. Decl., ¶¶ 281-282.

b. Limitation [17.2]

Halbert discloses Limitation [17.2]. Halbert discloses that "[m]odule controller 110 synchronizes the operation of the data port buffer 122, MUX/DeMUX 124, and data registers 126 and 128 via a number of control signals. For instance, direction signal DIR specifies whether data flow is towards the memory array (TO) or away from the memory array (AWAY)." Halbert, [0034]. As shown in Fig. 5 below, the set of consecutively transmitted data bits, i.e., DO_a1 and DO_b1, are successively transferred through the circuit 120 in response to the DIR control signal going high at a quarter clock cycle after T6.



Halbert, Fig. 5; Decl., ¶ 283.

4. Claim 18

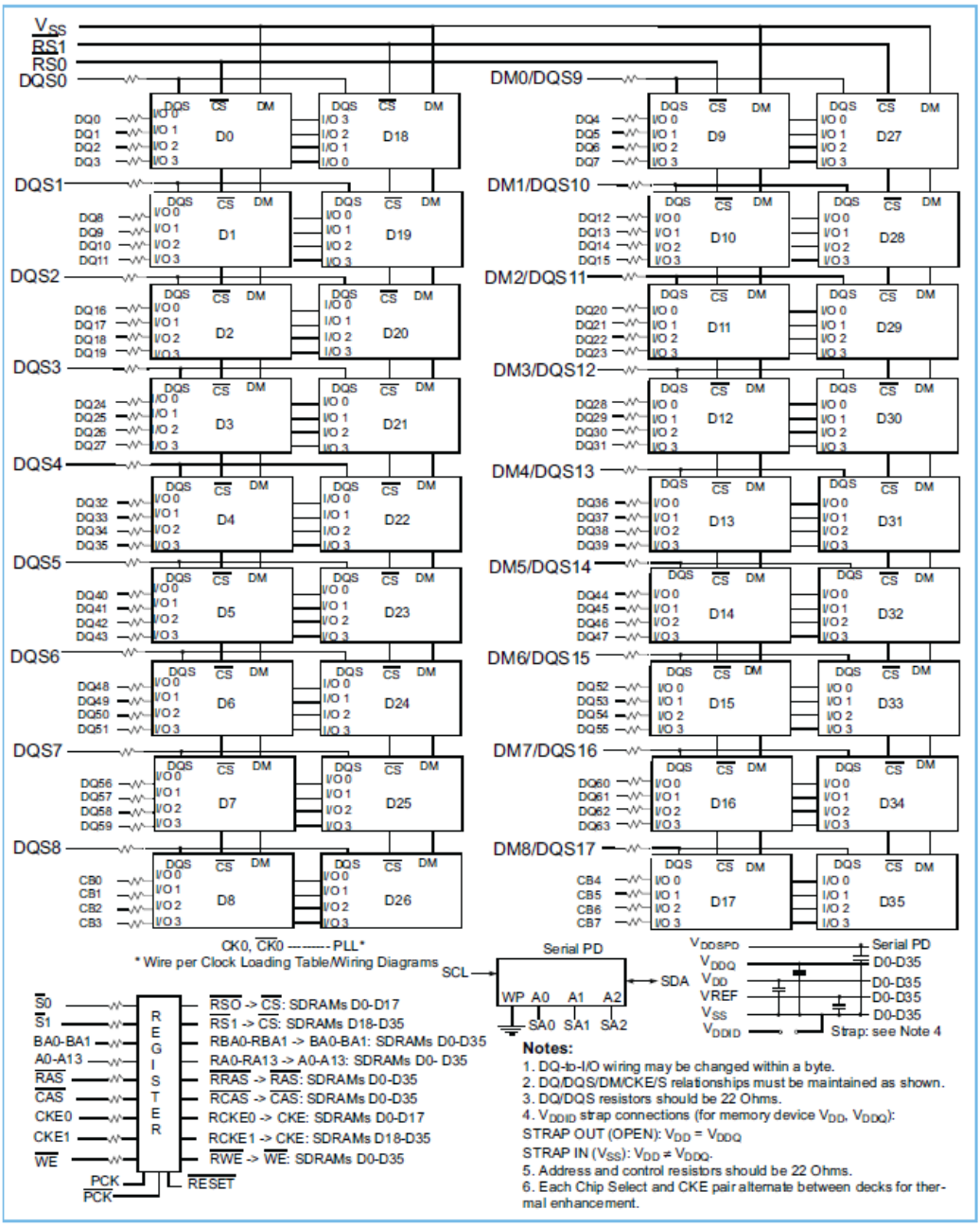
a. Limitations [18.1] and [18.2]

Claim 18 depends on claim 15. Halbert discloses Limitations [18.1] and [18.2]. Halbert discloses that "[t]he types, sizes, or numbers of memory devices selected for use with the present invention are not critical" (Halbert, [0061]) and that in memory device banks, "[a] total of nB DQ lines carry data signals, where B is the number of devices in one bank (e.g., eight or nine), and n is the data width of each device (e.g., four, eight, or sixteen bits)" (*Id*., [0009]). Thus, it would have been obvious that the memory devices of memory device ranks 140 and 142 could each be 4-bits wide. Decl., ¶¶ 285-286. Moreover, it would have been obvious that

memory device ranks 140 and 142 could each contain 18 devices configured in pairs with four-bit data widths to provide for 72-bit-wide data transfers. Decl., ¶ 289.

To the extent Halbert does not teach this limitation, it would have been obvious in view of JESD21-C. As shown in Card N below, JESD21-C discloses two physical banks of x4 DDR SDRAMs.

Block Diagram: Raw Card Version N (Populated as two physical banks of x4 DDR SDRAMs)



JESD21-C, 15. The first physical bank of x4 DDR SDRAM has 18 memory devices, e.g., D0-D17, each 4-bits wide, e.g., I/O0-I/O3, arranged in pairs, e.g., DQ0-DQ3 on D0 and DQ4-DQ7 on D9, DQ8-DQ11 on D1 and DQ12-DQ15 on D10, etc. Likewise, Card N discloses a second physical bank of x4 DDR SDRAM that has 18

memory devices, e.g., D18-D35, each 4-bits wide, e.g., I/O0-I/O3, arranged in pairs, e.g., DQ0-DQ3 on D18 and DQ4-DQ7 on D27, DQ8-DQ11 on D19 and DQ12-DQ15 on D28, etc. Thus, JESD21-C discloses a plurality of ranks that includes 18 4-bit wide memory devices configured in pairs to provide for 72-bit-wide data transfers. Decl., ¶¶ 287, 290.

Furthermore, D0 and D9 are an example pair of memory devices from the first physical bank (rank) that communicate on DQ0-DQ3 and DQ4-DQ7, respectively, providing a total of 8 bits, i.e., a byte, of the 72-bit wide memory rank, i.e., D0-D17. Decl., ¶ 291. A POSITA would have understood that this pair of memory devices D0 and D9 are configured to simulate an 8-bit wide memory device because they communicate using 8-bit wide data transfers. *Id*. Each pair from the first rank can communicate in this manner. *Id*.

D18 and D27 are an example pair of memory devices from the second physical bank (rank) that communicate on DQ0-DQ3 and DQ4-DQ7, respectively, providing a total of 8 bits, i.e., a byte, of the 72-bit wide memory rank, i.e., D18-D35. Decl., ¶ 292. A POSITA would have understood that this pair of memory devices D18 and D27 are configured to simulate an 8-bit wide memory device because they communicate using 8-bit wide data transfers. *Id*. Each pair from the second rank can communicate in this manner. *Id*.

A POSITA would have been motivated to combine the teachings of JESD21-C with Halbert for at least the reasons specified above. *See* §V.B.1.d; Decl., ¶ 288, 293.

5. Claim 19

Claim 19 depends on claim 15. Halbert in view of JESD21-C would have rendered the limitation of Claim 19 obvious. Halbert discloses that "[t]he illustrated examples also show two ranks of memory, but *other numbers of ranks are also possible, e.g., a 4:1 multiplexer and four ranks of memory*." Halbert, [0058] (emphasis added); Decl., ¶¶ 295-296.

Furthermore, JESD21-C discloses in the Pin Description that the first set of input address and control signals could include four chip selects, one for each of the four ranks.

Pin Description

Pin Name	Description	Pin Name	Description
A0 - A15	SDRAM address bus	CK0	SDRAM clock (positive line of differential pair)
BA0 - BA1	SDRAM bank select	$\overline{CK0}$	SDRAM clock (negative line of differential pair)
DQ0 - DQ63	DIMM memory data bus	SCL	IIC serial bus clock for EEPROM
CB0 - CB7	DIMM ECC check bits	SDA	IIC serial bus data line for EEPROM
$\overline{RAS}$	SDRAM row address strobe	SA0 - SA2	IIC slave address select for EEPROM
$\overline{CAS}$	SDRAM column address strobe	V_{DD}	SDRAM positive power supply
$\overline{WE}$	SDRAM write strobe	V_{DDQ}	SDRAM I/O Driver positive power supply
$\overline{S0}$ - $\overline{S3}$	SDRAM chip select lines (Physical. banks 0, 1, 2, and 3)	V_{REF}	SDRAM I/O reference supply
CKE0 - CKE1	SDRAM clock enable lines	V_{SS}	Power supply return (ground)
DQS0 - DQS8	SDRAM low data strobes	V_{DDSPD}	Serial EEPROM positive power supply (Supports both 2.5 Volt and 3.3 Volt operation)
DM(0-8)/DQS(9-17)	SDRAM low data masks/high data strobes (x4, x8-based x72 DIMMs)	NC	Spare Pins (no connect)
V_{DDID}	V_{DD} Identification Flag	$\overline{RESET}$	Reset pin (forces register inputs low)
Test	Used by memory bus analysis tools (unused on memory DIMMs)		

JESD21-C, 6 (annotated). As disclosed in the Pin Description above, S0-S3[bar] are "SDRAM chip select lines (Physical. Banks 0, 1, 2, and 3)." *Id.* S0[bar] is for selecting rank 0, S1[bar] is for selecting rank 1, S2[bar] is for selecting rank 2, and S3[bar] is for selecting rank 3. Thus, a POSITA would have understood that the first set of input address and control signals could include four chip select signals, one for each of the four ranks. Decl., ¶ 297.

A POSITA would have been motivated to combine the teachings of JESD21-C with Halbert for at least the reasons specified above. *See* §V.B.1.d; Decl., ¶ 298.

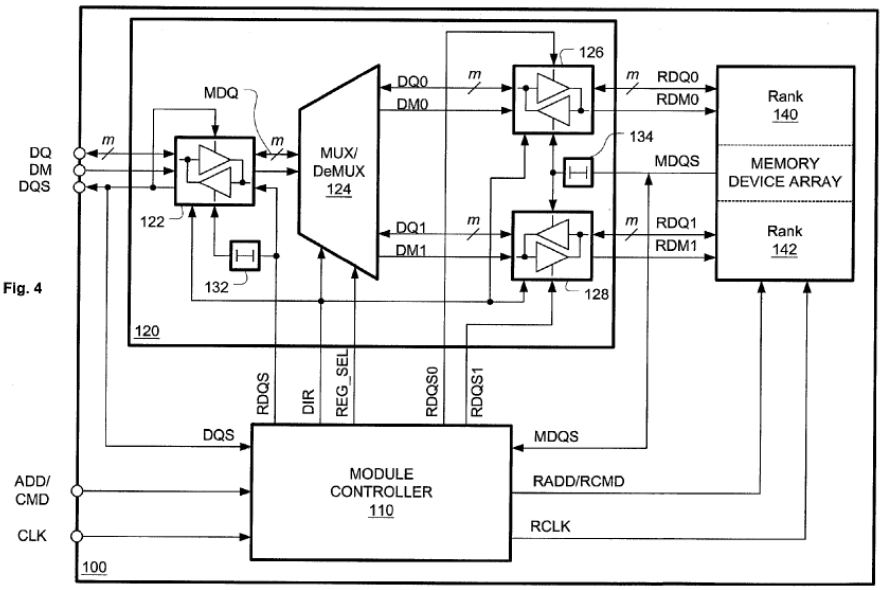
6. Claim 20

Claim 20 depends on claim 15. Halbert discloses the limitation of Claim 20. Data transfer through register 126 is one pipeline and through register 128 is a second pipeline. Halbert discloses that "[i]n FIG. 4, either data signals DQ0 (from register 126) or data signals DQ1 (from register 128) can be multiplexed to buffer 122 when the module is reading from memory device array 140/142. Likewise, when the module is writing to the memory device array, data signals MDQ from buffer 122 can be channeled to either DQ0 or DQ1." Halbert, [0033]. Thus, Halbert discloses that data interface circuit 120 includes logic pipelines, i.e., the circuit paths from buffer 122 through MUX/DeMUX 124 through either register 126 or register 128, that enable data transfers between memory device rank 140 and memory bus 22 through the circuitry in response to the first control signals associated with the

read operation/command, by multiplexing data signal DQ0 from register 126 to buffer 122. Decl., ¶¶ 300-301.

7. Claim 22

Claim 22 depends on claim 15. Halbert discloses the limitation of Claim 22. Halbert discloses that "one embodiment describes a DIMM that can, with the same type of devices, number of devices, and data signal pins as the dual-bank registered DIMM, provide twice the data rate of the registered DIMM." Halbert, [0024]. A POSITA would have understood that Halbert's memory module 100 enables data and data strobes transfer from the memory device rank 140 to memory controller 20 in response to the read command at the specified data rate, i.e., at twice the data rate of the registered DIMM. Decl., ¶¶ 303-304; *see also* Halbert, [0035] (describing the AWAY (read) mode). As shown in Fig. 4 below, the first burst of data and first burst of data strobes are transferred between the first N-bit wide rank (memory device array 140) and the memory controller (to the left of Fig. 4 on DQ).



Halbert, Fig. 4 (showing RDQ0 from memory device rank 140 and DQ out to the memory controller); *see also id*., [0030]-[0031], [0038]; Decl., ¶ 305.

8. Claim 23

a. Limitation [23.1]

Claim 23 depends on claim 15. Halbert discloses Limitation [23.1]. Halbert discloses that "[i]n a registered DIMM, the system clock CK0 is received by phase-locked-loop (PLL) 27, which creates a set of module clock signals." Halbert, [0009]. The system clock CK0 signal is sent from the memory controller to the PLL, which in response, outputs a set of module clock signals. Decl., ¶¶ 307-308.

Halbert further discloses that "a primary memory controller initiates READ operations [for memory module 100] just like it would for a registered DIMM." Halbert, [0037]. Memory Module 100 is just another design of a registered DIMM. Thus, it would have been obvious to have the memory controller send the system

clock CK0 to a PLL to output clock signals, i.e., a set of module clock signals, for memory module 100. Decl., ¶ 309.

b. Limitation [23.2]

Halbert discloses Limitation [23.2]. As discussed above for Limitation [15.12], Halbert discloses that data interface circuit 120 is configured to add a predetermined time delay of one clock cycle for each registered data transfer. *See* §V.B.1.l. It would have been obvious to a POSITA that registers 126 and 128 could each be configured to add a one clock cycle time delay. *See, e.g.*, Halbert, [0010] (Signals pass through a register with a one clock cycle time delay. "Register 25 latches these signals, and places them on the module bus at T2. After a known RAS (row address strobe) latency, the controller transmits a READ command along with a COL 'a' address. These signals also pass through register 25 with a one-clock cycle delay."); *see also* JESD21-C, 68; Decl., ¶ 310.

9. Claim 24

a. Limitation [24.1]

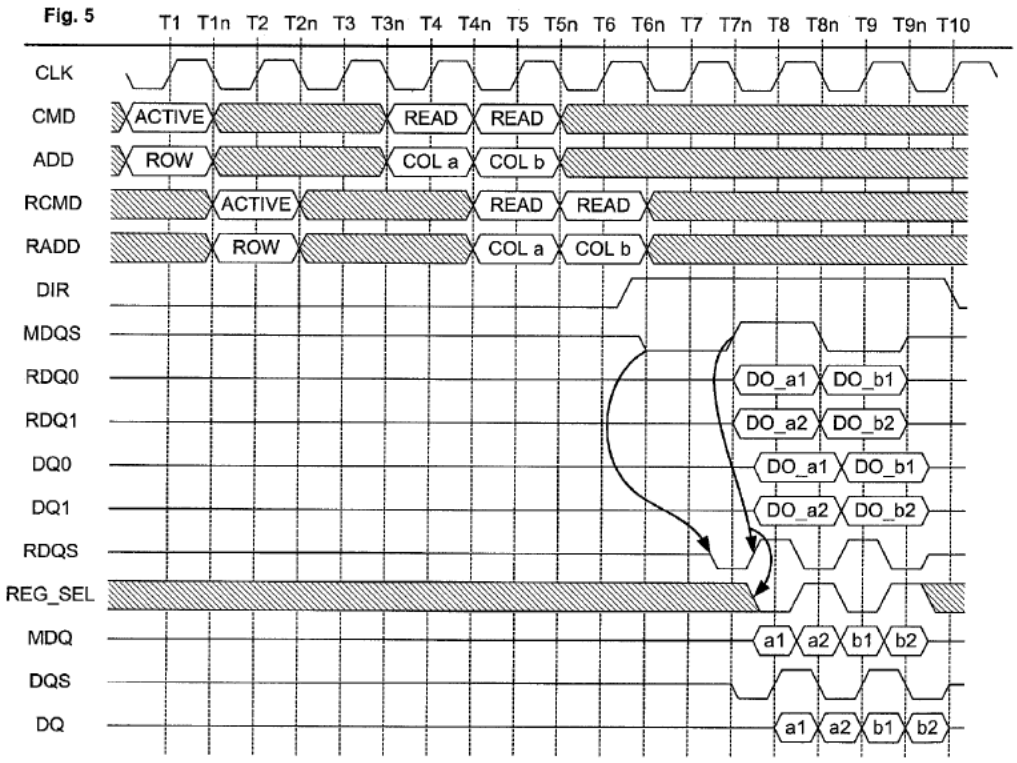
Claim 24 depends on claim 23. Halbert discloses Limitation [24.1]. Halbert discloses that the "types, sizes, or numbers of memory devices selected for use with the present invention are not critical. Some possible device types include dynamic random access memory (DRAM) devices, *synchronous DRAM (SDRAM) devices*." Halbert, [0061] (emphasis added). Moreover, Halbert discloses that the SDRAM is configured to operate synchronously with the clock signal by the module controller

110. "The module controller 110 synchronizes the operation of module 100 with the attached memory system." *Id*., [0029]; Decl., ¶¶ 312-313.

b. Limitation [24.2]

Halbert discloses Limitation [24.2]. Halbert discloses that "[d]evice array 140/142 signifies that it is about to drive data onto buses RDQ0 and RDQ1 by taking data strobe MDQS low at T6n." Halbert, [0038]. Thus, device array 140 is configured to output data onto bus RDQ0. Decl., ¶ 314.

The data is output on both edges of the respective set of data strobes of the first burst of data strobes. Referring to Fig. 5 below, the first burst of N-bit wide data signals from memory device 140, i.e., DO_a1 and DO_b1, is output onto RDQ0 at T7n and T8n, respectively. DO_a1 is output on the rising edge of the respective set of data strobes of the first burst of data strobes, i.e., MDQS, at T7n, and DO_b1 is output on the falling edge of MDQS at T8n.



Halbert, Fig. 5; Decl., ¶ 315.

10. Claim 25

a. Limitation [25.1]

Claim 25 depends on claim 15. Halbert discloses Limitation [25.1]. As discussed above for Limitation [15.3], the logic, module controller 110, "can provide … registered versions of address and command signals, RADD/RCMD" in response to receipt of "[a]ddress and command signals ADD/CMD." Halbert, [0029], [0009]. This happens in module controller 110 shown in Fig. 4.

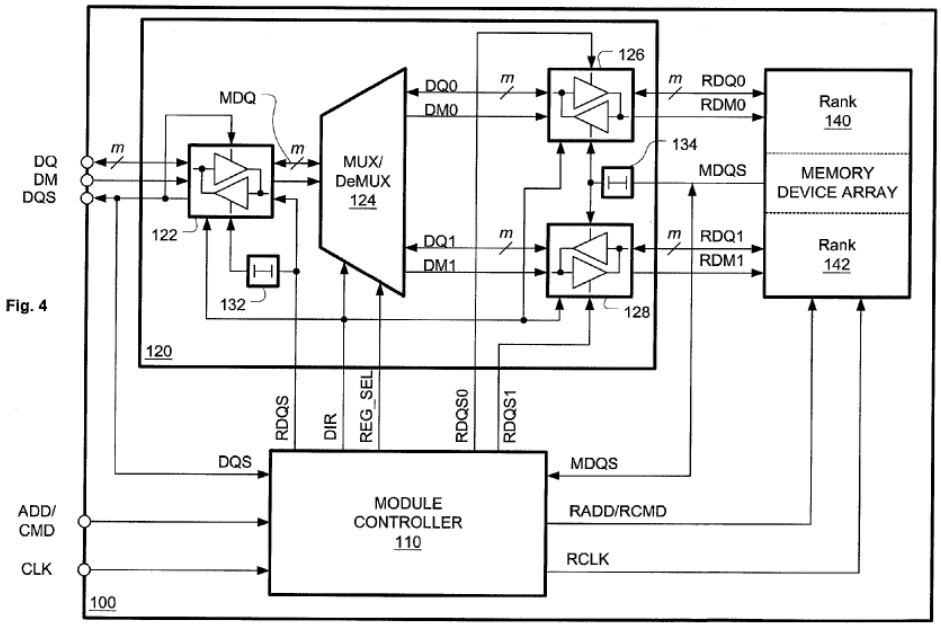


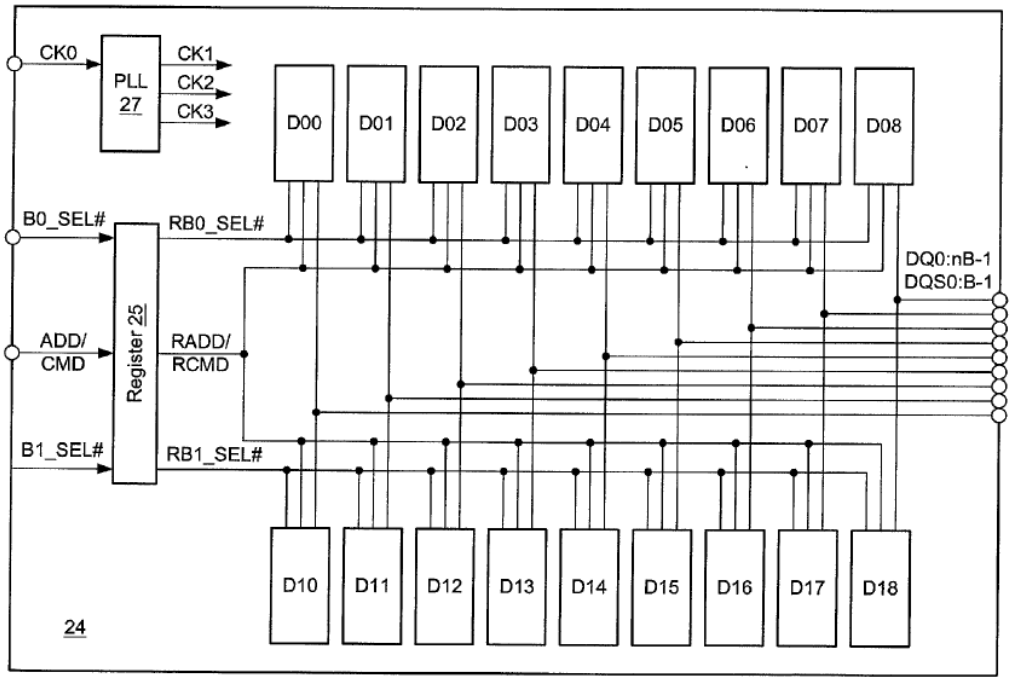
Fig. 4

Halbert, Fig. 4; Decl., ¶¶ 317-319. Fig. 4 shows a second set of input address and control signals, i.e., ADD/CMD, which is associated with the write command, input into module controller 110 and a second set of registered address and control signals, i.e., RADD/RCMD, output from the module controller 110. *See also* Halbert, Fig. 6 (showing RCMD and RADD); Decl., ¶ 319.

b. Limitation [25.2]

Halbert discloses Limitation [25.2]. In describing registered DIMM designs, as depicted in Fig. 2 below, Halbert discloses that there are "two bank select signals, B0_SEL# and B1_SEL#, each pass[ing] through register 25 and connect[ing] to a chip select pin on a corresponding one of the banks of memory devices." Halbert, [0009].

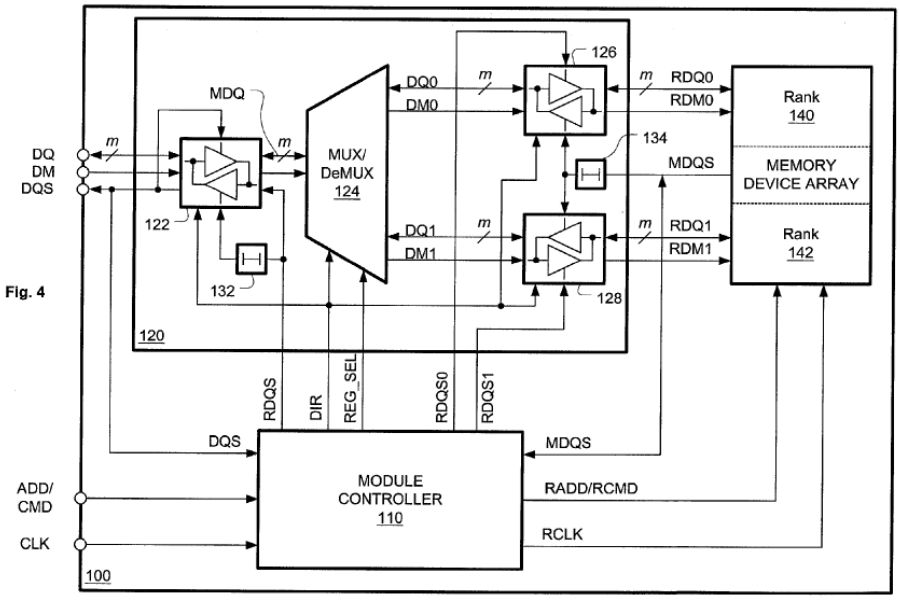
Fig. 2
(Prior Art)



Id., Fig. 2. B0_SEL# and B1_SEL# are a second plurality of input chip select signals corresponding to the D00-D08 and D10-D18 memory ranks, respectively, and are part of the second set of input address and control signals for the write operation, i.e., ADD/CMD. Decl., ¶ 320.

Referring to Fig. 4 below, it would have been obvious to a POSITA to include the second plurality of input chip select signals B0_SEL# and B1_SEL# with the ADD/CMD signals sent by the same memory controller to module controller 110, similar to B0_SEL# and B1_SEL# input to register 25 in Fig. 2, to correspond to memory device ranks 140 and 142, respectively, because Halbert discloses, e.g., "a primary memory controller initiates [] operations [for memory module 100] just like it would for a registered DIMM." Halbert, [0037]. Memory Module 100 is just

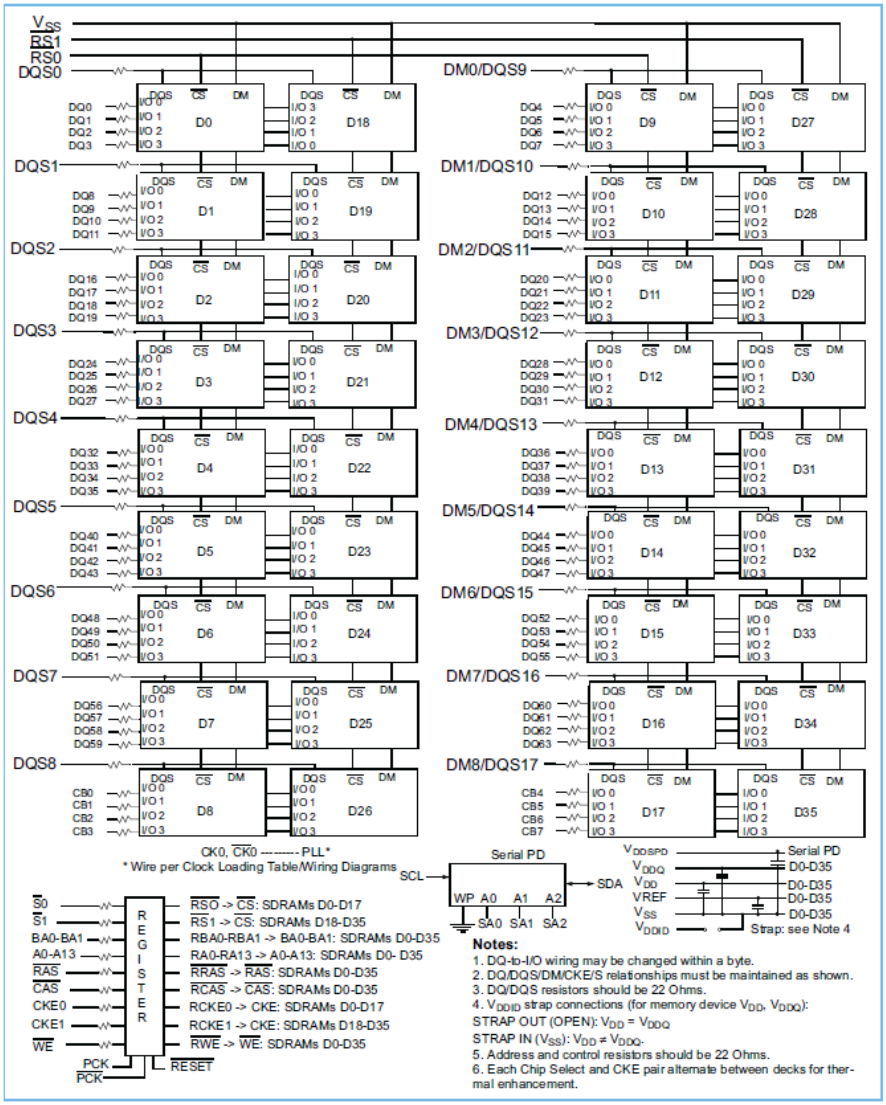
another design of a registered DIMM, so it would have been obvious to include B0_SEL# and B1_SEL# with the ADD/CMD signals of Fig. 4. Decl., ¶ 321. Module controller 110 in Fig. 4 would have a set of chip selects as inputs because there are multiple memory device ranks 140 and 142, and there would be chip selects to select whether data is transferred to/from memory device rank 140 or 142.



Id., Fig. 4; Decl., ¶ 321.

To the extent Halbert does not teach this limitation, it would have been obvious in view of JESD21-C. JESD21-C discloses a second plurality of input chip select signals S0 and S1 input to the register, as shown in Card N below. Chip select S0 corresponds to the rank that includes the D0-D17 memory devices, and chip select S1 corresponds to the rank that includes the D18-D35 memory devices.

Block Diagram: Raw Card Version N (Populated as two physical banks of x4 DDR SDRAMs)



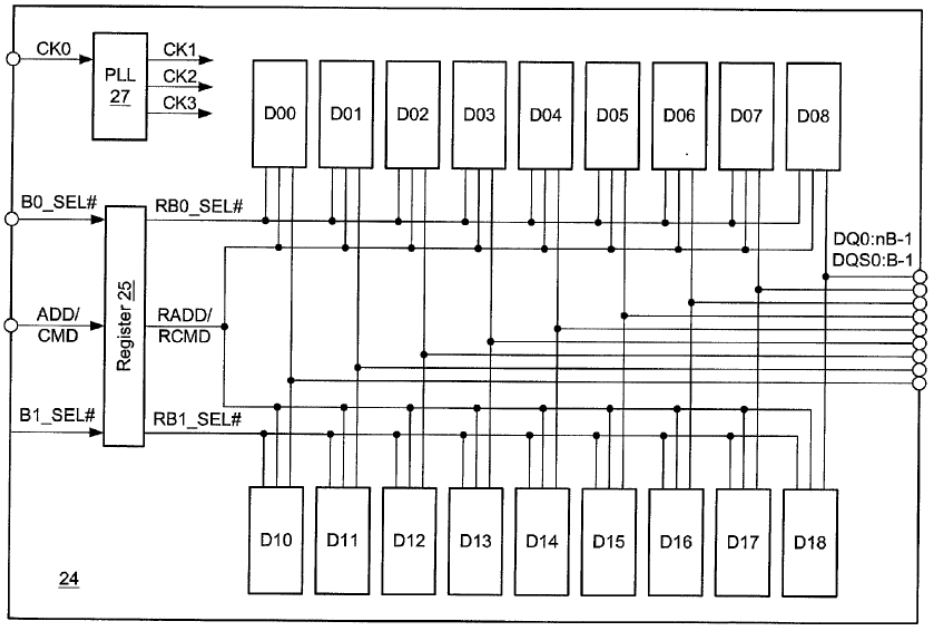
JESD21-C, 15; Decl., ¶ 322. JESD21-C's Card N discloses a block diagram of two physical banks of x4 DDR SDRAMs, which is what is disclosed in Fig. 4 of Halbert, i.e., memory device ranks 140 and 142. Thus, like Fig. 2 in Halbert, there would be a second plurality of chip selects input to module controller 110 in Fig. 4. *Id.*

A POSITA would have been motivated to combine the teachings of JESD21-C with Halbert for at least the reasons specified above. *See* §V.B.1.d; Decl., ¶ 323.

c. Limitation [25.3]

Halbert discloses Limitation [25.3]. Halbert discloses that the "two bank select signals, B0_SEL# and B1_SEL#, each pass through register 25 and connect to a chip select pin on a corresponding one of the banks of memory devices." Halbert, [0009]. Thus, along with the second set of registered address and control signals, i.e., RADD/RCMD, Halbert discloses RB0_SEL# and RB1_SEL# as a second plurality of registered chip select signals that correspond to the second plurality of input chip select signals, i.e., B0_SEL# and B1_SEL#, respectively, as shown in Fig. 2 below.

Fig. 2
(Prior Art)



Id., Fig. 2; Decl., ¶ 324.

Referring to Fig. 4 below, it would have been obvious to a POSITA to include the second plurality of registered chip select signals RB0_SEL# and RB1_SEL# that

correspond to the second plurality of input chip select signals B0_SEL# and B1_SEL#, respectively, with the RADD/RCMD signals output by module controller 110, similar to RB0_SEL# and RB1_SEL# output from register 25 in Fig. 2, because Halbert discloses, e.g., "a primary memory controller initiates [] operations [for memory module 100] just like it would for a registered DIMM." Halbert, [0037]; Decl., ¶ 325. Memory Module 100 is just another design of a registered DIMM, so it would have been obvious to include RB0_SEL# and RB1_SEL# with the RADD/RCMD signals of Fig. 4. *Id*. Module controller 110 in Fig. 4 would have a plurality of registered chip selects as outputs because there are multiple memory device ranks 140 and 142, and there would be registered chip selects to select whether data is transferred to/from memory device rank 140 or 142.

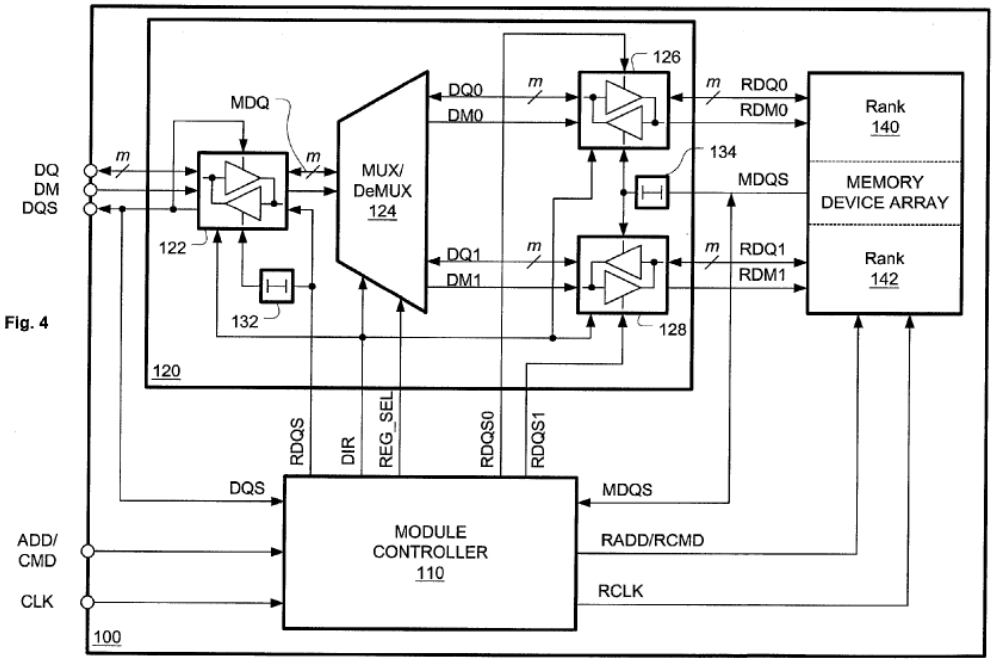
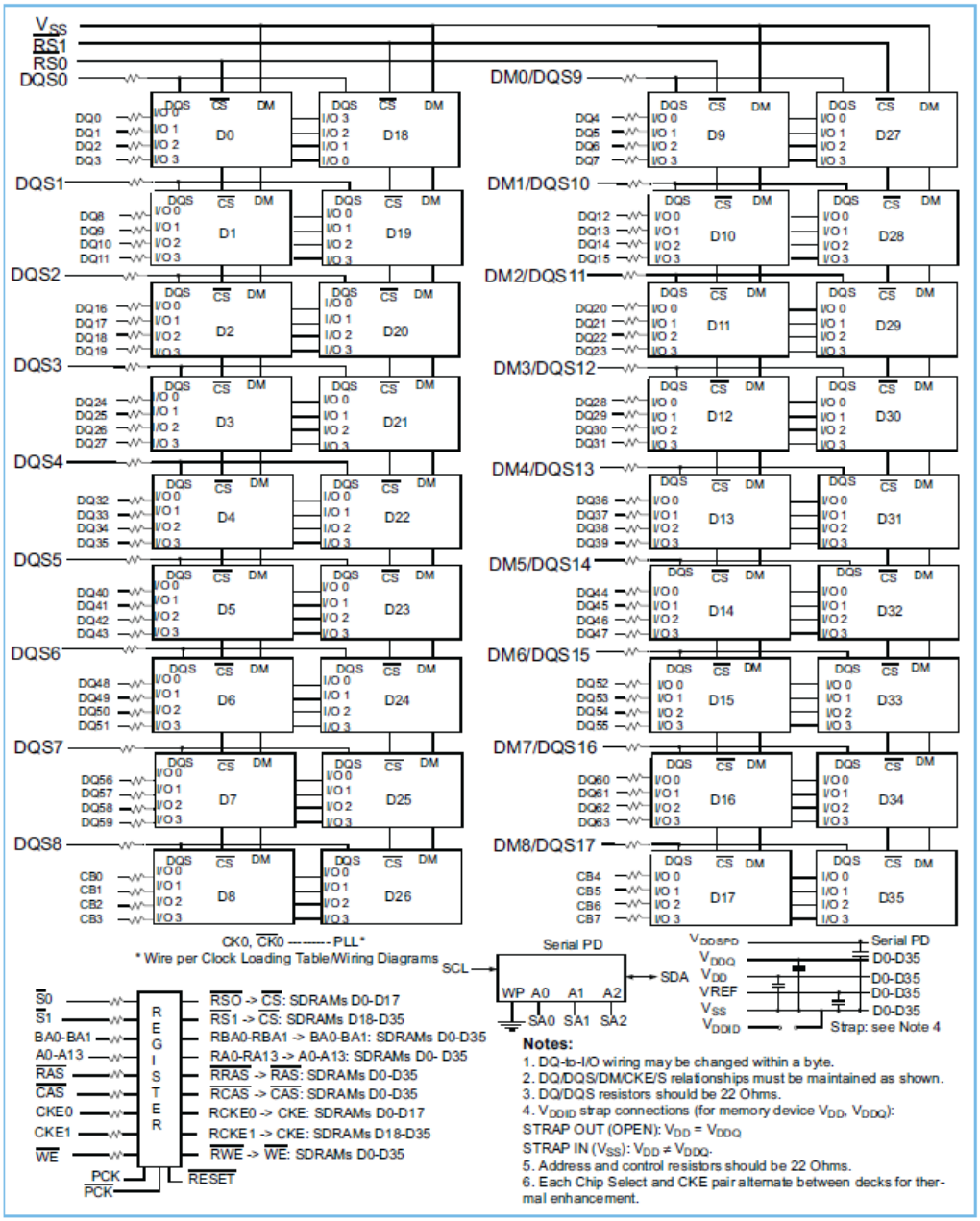


Fig. 4

Halbert, Fig. 4; Decl., ¶ 325.

To the extent Halbert does not teach this limitation, it would have been obvious in view of JESD21-C. JESD21-C discloses a second plurality of registered chip select signals RS0 and RS1 output from the register, as shown in Card N below. RS0 and RS1 correspond to the second plurality of input chip select signals S0 and S1 and are shown as input to each bank of memory ranks. Registered chip select RS0 corresponds to the D0-D17 memory ranks, and registered chip select RS1 corresponds to the D18-D35 memory ranks.

Block Diagram: Raw Card Version N (Populated as two physical banks of x4 DDR SDRAMs)



JESD21-C, 15; Decl., ¶ 326. JESD21-C's Card N discloses a block diagram of two physical banks of x4 DDR SDRAMs, which is what is disclosed in Fig. 4 of Halbert, i.e., memory device ranks 140 and 142. Thus, like Fig. 2 in Halbert, there would be

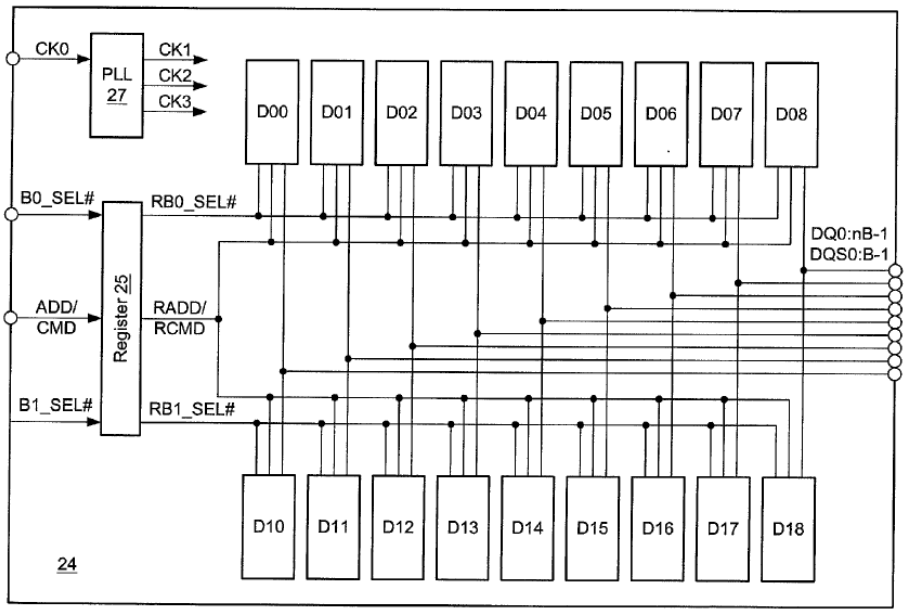
a second plurality of registered chip selects output from module controller 110 in Fig. 4 that correspond to the second plurality of input chip select signals. *Id.*

A POSITA would have been motivated to combine the teachings of JESD21-C with Halbert for at least the reasons specified above. *See* §V.B.1.d; Decl., ¶ 327.

d. Limitation [25.4]

Halbert discloses Limitation [25.4]. As discussed above, Halbert discloses a second plurality of registered chip select signals RB0_SEL# and RB1_SEL#. Referring to Fig. 2 below, RB1_SEL# has an active signal value when selecting the D10-D18 memory ranks for data transfers. When RB1_SEL# has an active signal value, RB0_SEL# has a non-active signal value because the D00-D08 memory ranks are not selected for data transfers.

Fig. 2
(Prior Art)



Halbert, Fig. 2; Decl., ¶ 328.

RB1_SEL# having an active signal value while RB0_SEL# has a non-active signal value can be explained with reference to Fig. 3 below.

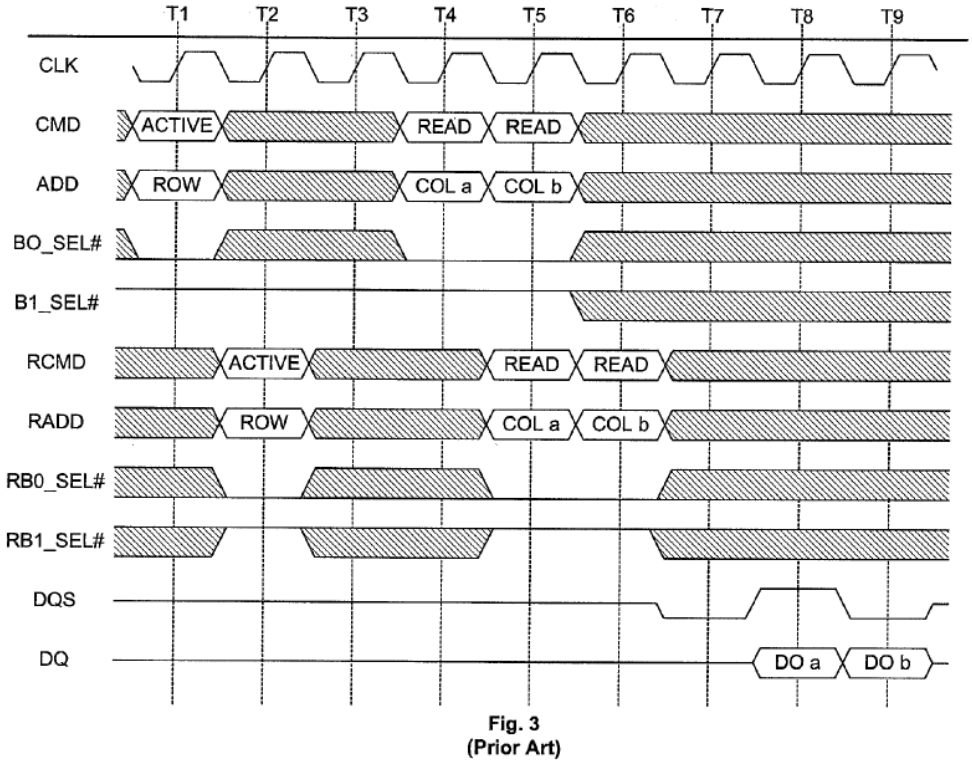


Fig. 3
(Prior Art)

Halbert, Fig. 3. While Fig. 3 is the timing diagram for two consecutive read operations, the RB1_SEL# and RB0_SEL# operate in the same manner for the write operation. Decl., ¶ 329. For the write operation, the signal for RB0_SEL# in Fig. 3 could have the signal for RB1_SEL# instead, and the signal for RB1_SEL# in Fig. 3 could have the signal for RB0_SEL# instead. *Id.* RB1_SEL# would then be low to indicate that it has an active signal value at all times the registered address and control signals are active, while RB0_SEL# would be high to indicate that it has a non-active signal value during those times. *Id.*

e. Limitation [25.5]

Halbert discloses Limitation [25.5]. As discussed above for Limitation [25.4], if RB1_SEL# has the active signal value and RB0_SEL# has the non-active signal value, then a second rank different from the first rank is configured to receive the second registered chip select signal having the active signal value, e.g., memory device rank 142 is active while memory device rank 140 is non-active. Decl., ¶ 330.

Halbert discloses that memory device rank 142 can be configured to receive the second burst of N-bit wide data signals and a second burst of data strobes associated with the write command. "[W]hen the module is writing to the memory device array, data signals MDQ from buffer 122 can be channeled to either DQ0 or DQ1," which is received by memory device rank 140 or 142, respectively. Halbert, [0033]. DQ1 is received at memory device array 142 on bus RDQ1. *See id*., [0036] ("Controller 110 strobes the memory device array, using the memory data strobe MDQS, to signal the array to write data from buses RDQ0 and RDQ1."); Decl., ¶ 331.

If memory device array 142 is the active rank, memory device array 142 receives the second burst of N-bit wide data signals, which occurs in response to the write command. "Upon sensing the first WRITE command, module controller 110 transitions to a WRITE state." Halbert, [0043]. Data signal on DQ1 is received by memory device array 142. "In the TO mode, register data strobes RDQS0 and

RDQS1 are also functional. … In the following bus clock cycle, m bits are directed to register 128 by strobing RDQS1. Both register contents are then written to memory device array 140/142 during a single device write cycle." *Id*., [0036], Fig. 6. Memory device array 142 also receives a second burst of data strobes, i.e., memory data strobe MDQS, as part of the write operation. "Controller 110 strobes the memory device array, using the memory data strobe MDQS, to signal the array to write data from buses RDQ0 and RDQ1." *Id*., [0036]; Decl., ¶ 332.

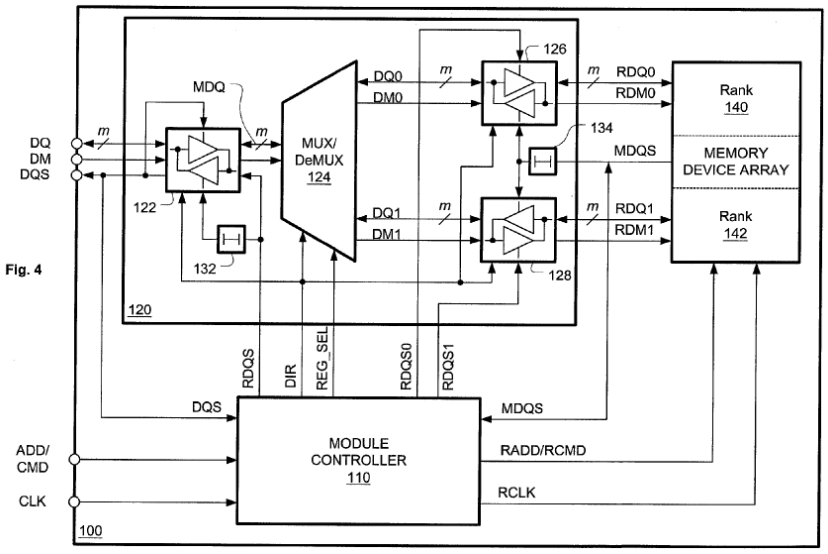
f. Limitation [25.6]

Halbert discloses Limitation [25.6]. As discussed above for Limitation [15.3], Halbert discloses that "[m]odule controller 110 synchronizes the operation of the data port buffer 122, MUX/DeMUX 124, and data registers 126 and 128 via a number of control signals. For instance, direction signal DIR specifies whether data flow is towards the memory array (TO) or away from the memory array (AWAY)." Halbert, [0034]. When data flow is towards the memory array, the logic, i.e., module controller 110, is responding to the second write command by outputting second control signals, i.e., TO, to the circuitry, i.e., data interface circuit 120. Decl., ¶ 333.

g. Limitation [25.7]

Halbert discloses Limitation [25.7]. As depicted in Fig. 4 below, Halbert discloses registers 126, 128, and 122 for providing registered data transfers through

data interface circuit 120. Register 128 provides the registered data transfers between the second rank, i.e., memory device rank 142, and the memory bus 22.

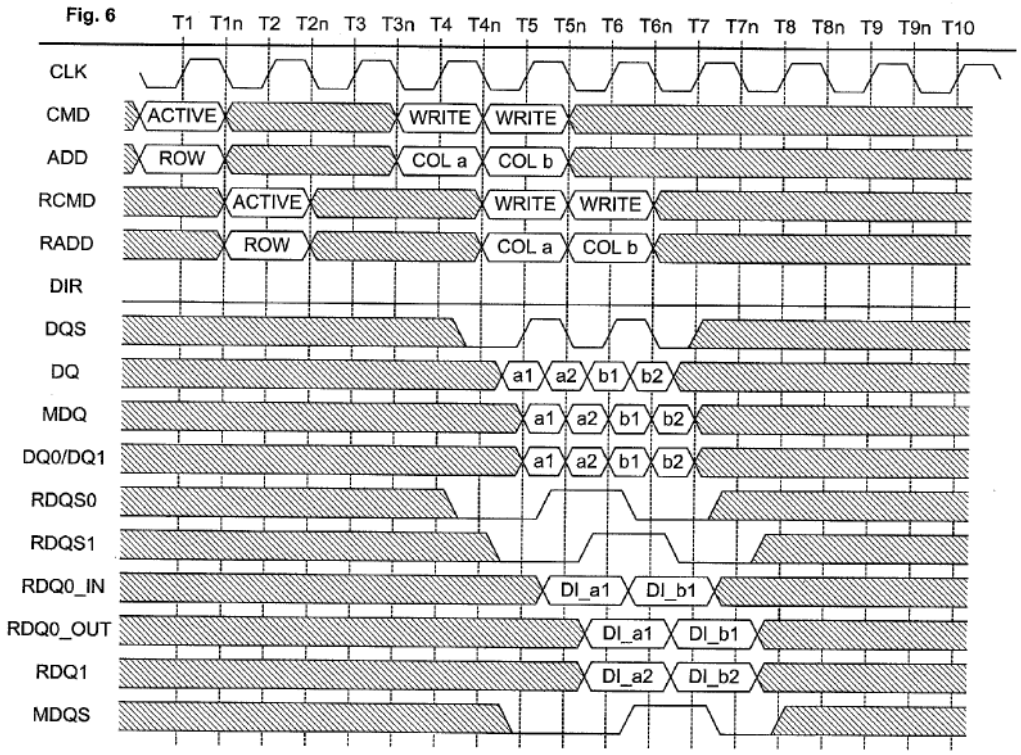


Halbert, Fig. 4; Decl., ¶ 334. "[W]hen the module is writing to the memory device array, data signals MDQ from buffer 122 can be channeled to … DQ1." Halbert, [0033]; *see also id*., [0036] ("In the TO mode, REG_SEL determines which of registers 126 and 128 will receive DQ at each memory bus clock cycle.").

Halbert further discloses that the second burst of N-bit wide data signals and the second burst of data strobes are transferred between memory device rank 142 and the memory controller 20 through the circuitry *in accordance with the overall CAS latency* of memory module 100. "The module controller 110 synchronizes the operation of module 100 with the attached memory system. Like the address/command registers and PLL of a registered DIMM, controller 110 can provide clock adjustment to an input CLK signal and registered versions of address

and command signals, RADD/RCMD. In addition, module controller 110 provides timing and synchronization signals to data interface circuit 120." Halbert, [0029]. A POSITA would have understood that module controller 110 provides all the necessary signals to synchronize the operation of memory module 100, including in accordance with the overall CAS latency of memory module 100. Decl., ¶ 335. In other words, a POSITA would have understood that because the data transfers occur within a timespan that would be considered the overall CAS latency of the memory module, the data transfers must be enabled in accordance with the overall CAS latency of the memory module. *Id*.; *see* §V.B.1.k.

Fig. 6 below shows a timing diagram for two consecutive write operations for the memory module of FIG. 4. The WRITE command for COL a is clocked in at T4 and data a1 and a2 are at the input of DQ at a quarter clock cycle after T4n and a quarter clock cycle after T5, respectively. Thus, Fig. 6 shows that the second burst of N-bit wide data signals and the second burst of data strobes (MDQS goes high a quarter clock cycle after T6) are transferred through data interface circuit 120 in accordance with the overall CAS latency of memory module 100, i.e., T4 to T8.

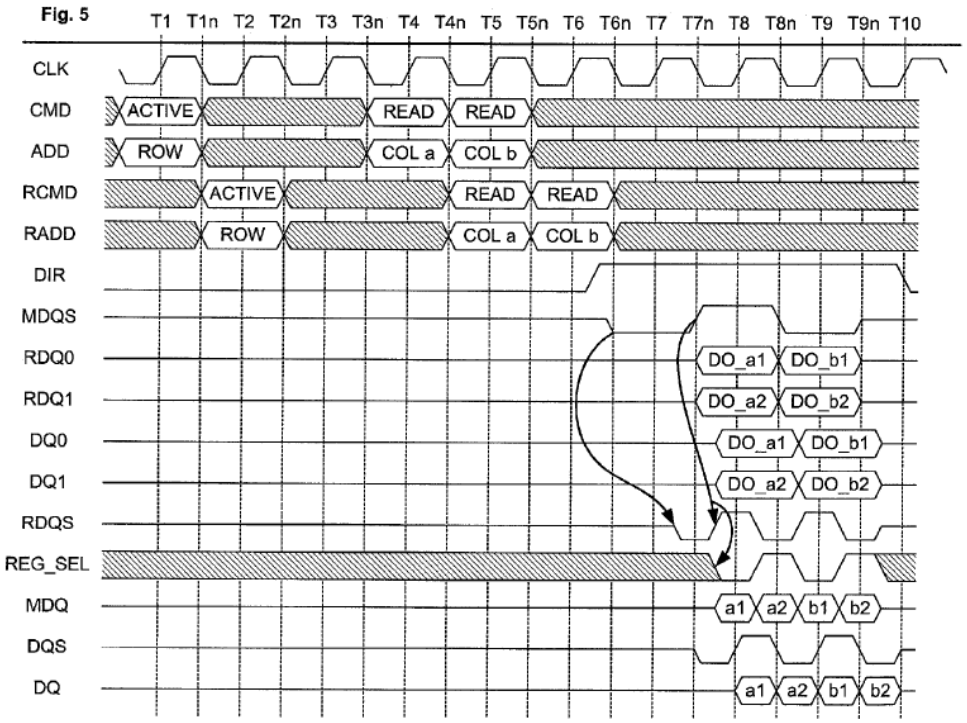


Halbert, Fig. 6; Decl., ¶ 336.

11. Claim 26

a. Limitation [26.1]

Claim 26 depends on claim 17. Halbert discloses Limitation [26.1]. Fig. 5 of Halbert "illustrates a timing diagram for two consecutive read operations (to the same ROW of the memory devices)." Halbert, [0037]. The read operation provides the first burst of N-bit wide data signals that is transferred through data interface circuit 120 during a plurality of time intervals including at least a first time interval and a last time interval, as shown in Fig. 5 below.



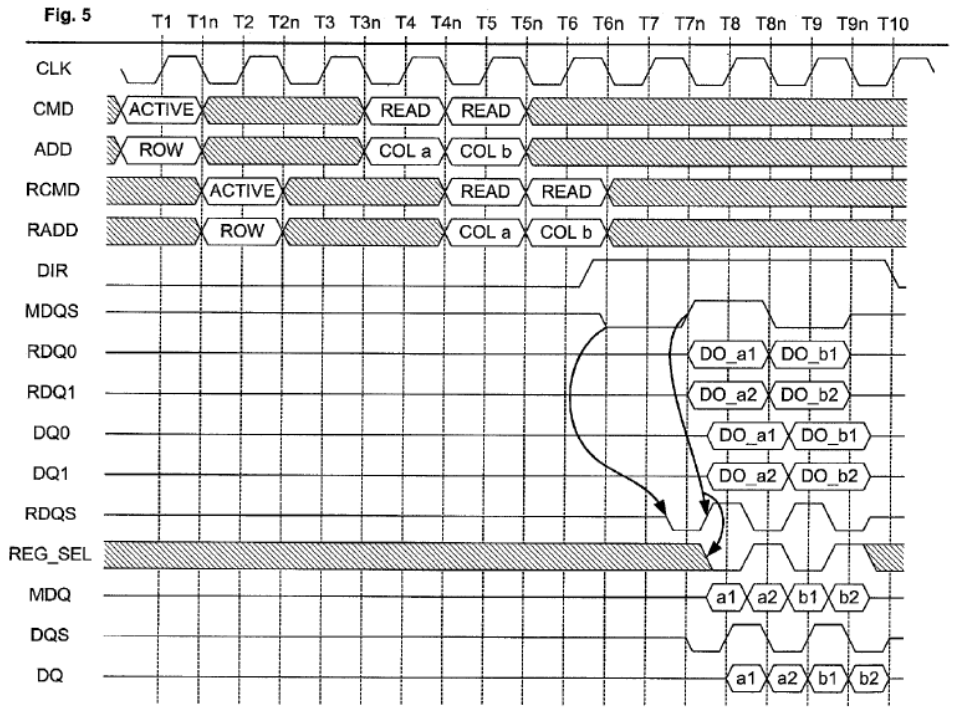
Id., Fig. 5; Decl., ¶¶ 338-339.

Referring to Fig. 5, Halbert discloses that "[a]t T 7n, device array 140/142 takes MDQS high, signifying that data outputs 'DO_a1' and 'DO_a2' are being driven respectively onto buses RDQ0 and RDQ1 at that time." Halbert, [0039]. Thus, as shown in Fig. 5, the first burst of N-bit wide data signals, i.e., DO_a1 and DO_b1 on RDQ0, is transferred through the circuitry in a plurality of time intervals including at least a first time interval, T7n-T8n, and a last time interval, T8n-T9n. Decl., ¶ 340.

b. Limitation [26.2]

Halbert discloses Limitation [26.2]. Control DIR enables the set of signal paths for receiving data from the memory array. "When DIR is set to AWAY, buffer

122 is configured as a driver, MUX/DeMUX 124 is configured as a MUX, and registers 126 and 128 are configured as receivers." Halbert, [0034]. Fig. 5 shows that control signal DIR enables a set of signal paths, e.g., RDQ0 and MDQS, in data interface circuit 120 before the first time interval (T7n-T8n), i.e., at a quarter clock cycle after T6 (which is before T7n), that is subsequently disabled after the last time interval (T8n-T9n), i.e., at T10 (which is after T9n).



Id., Fig. 5. Decl., ¶ 341.

12. Claim 27

a. Limitation [27.1]

Claim 27 depends on claim 26. Halbert discloses Limitation [27.1]. Halbert discloses that "[i]n FIG. 4, either data signals DQ0 (from register 126) or data signals

DQ1 (from register 128) can be multiplexed to buffer 122 when the module is reading from memory device array 140/142." Halbert, [0033]; *see also id*., Fig. 5 (showing READ on the CMD line); Decl., ¶¶ 343-344. Thus, Halbert discloses a first read memory command.

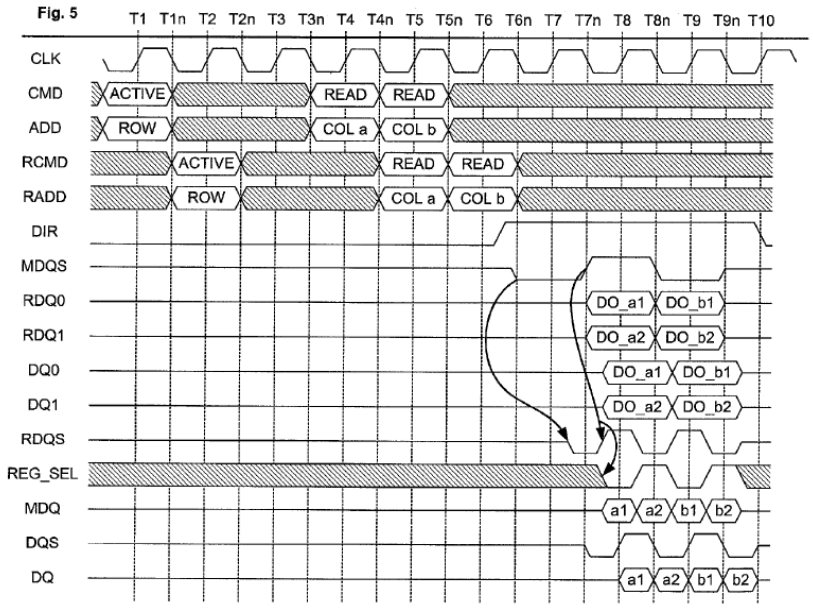
b. Limitation [27.2]

Halbert discloses Limitation [27.2]. Halbert discloses that "[i]n FIG. 4, … when the module is writing to the memory device array, data signals MDQ from buffer 122 can be channeled to either DQ0 or DQ1." Halbert, [0033]; *see also id*., Fig. 6 (showing WRITE on the CMD line); Decl., ¶ 345. Thus, Halbert discloses a second write memory command.

c. Limitation [27.3]

Halbert discloses Limitation [27.3]. Halbert discloses that the set of signal paths, i.e., RDQ0 and MDQS, are enabled to transfer the first burst of N-bit wide data signals and the first burst of data strobes, i.e., MDQS goes high, a first number of time intervals after the read memory command is received by the logic. Decl., ¶ 346.

Referring to Fig. 5 below, the read memory command is clocked into the logic at T4. MDQS goes high at T7n, which is a first number of time intervals, i.e., three-and-a-half clock cycles, after the read memory command.

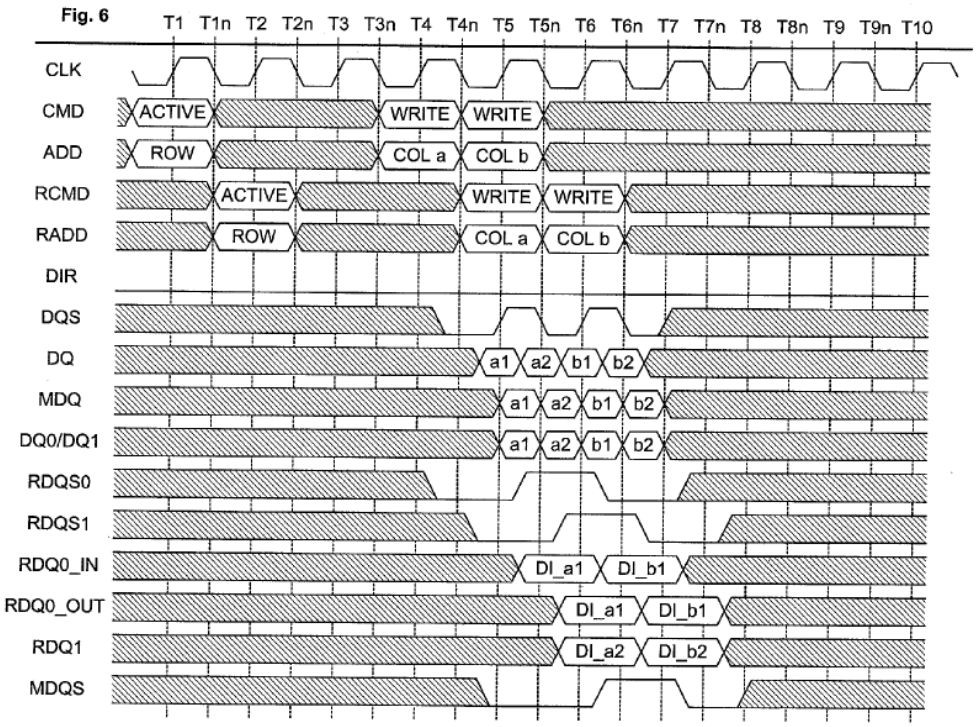


Halbert, Fig. 5; Decl., ¶ 347.

d. Limitation [27.4]

Halbert discloses Limitation [27.4]. Halbert discloses that the set of signal paths, i.e., RDQ1 and MDQS, are enabled to transfer the second burst of N-bit wide data signals and the second burst of data strobes, i.e., MDQS goes high, a second number of time intervals after the write memory command is received by the logic, the second number being different from the first number. Decl., ¶ 348.

Referring to Fig. 6 below, the write memory command is clocked into the logic at T4. MDQS goes high at a quarter clock cycle after T6, which is a first number of time intervals, i.e., two-and-a-quarter clock cycles, after the write memory command that is different from the three-and-a-half clock cycles for the read memory command.



Halbert, Fig. 6; Decl., ¶ 349.

13. Claim 28

a. Limitation [28.1]

Halbert discloses Limitation [28.1] for the same reasons discussed above for Limitation [15.1]. *See* §V.B.1.a; Decl., ¶¶ 352-357.

b. Limitation [28.2]

Halbert discloses Limitation [28.2] for the same reasons discussed above for Limitation [15.2]. *See* §V.B.1.b; Decl., ¶¶ 358-361.

c. Limitation [28.3]

Halbert discloses Limitation [28.3] for the same reasons discussed above for Limitation [15.3]. *See* §V.B.1.c; Decl., ¶¶ 362-363.

d. Limitation [28.4]

Halbert discloses Limitation [28.4] for the same reasons discussed above for Limitation [15.4]. *See* §V.B.1.d; Decl., ¶¶ 364-367.

e. Limitation [28.5]

Halbert discloses Limitation [28.5] for the same reasons discussed above for Limitation [15.5]. *See* §V.B.1.e; Decl., ¶¶ 368-371.

f. Limitation [28.6]

Halbert discloses Limitation [28.6] for the same reasons discussed above for Limitation [15.6]. *See* §V.B.1.f; Decl., ¶¶ 372-374.

g. Limitation [28.7]

Halbert discloses Limitation [28.7] for the same reasons discussed above for Limitation [15.7]. *See* §V.B.1.g; Decl., ¶¶ 375-376.

h. Limitation [28.8]

Halbert discloses Limitation [28.8] for the same reasons discussed above for Limitation [15.8]. *See* §V.B.1.h; Decl., ¶¶ 377-380.

i. Limitation [28.9]

Halbert discloses Limitation [28.9] for the same reasons discussed above for Limitation [15.9]. *See* §V.B.1.i; Decl., ¶¶ 381-382.

j. Limitation [28.10]

Halbert discloses Limitation [28.10] for the same reasons discussed above for Claim 20. *See* §V.B.6; Decl., ¶ 383.

k. Limitation [28.11]

Halbert discloses Limitation [28.11] for the same reasons discussed above for Limitation [15.11]. *See* §V.B.1.k; Decl., ¶¶ 384-387.

l. Limitations [28.12] and [28.13]

Halbert discloses Limitations [28.12] and [28.13] for the same reasons discussed above for Limitation [15.12]. *See* §V.B.1.l; Decl., ¶¶ 388-392.

14. Claim 29

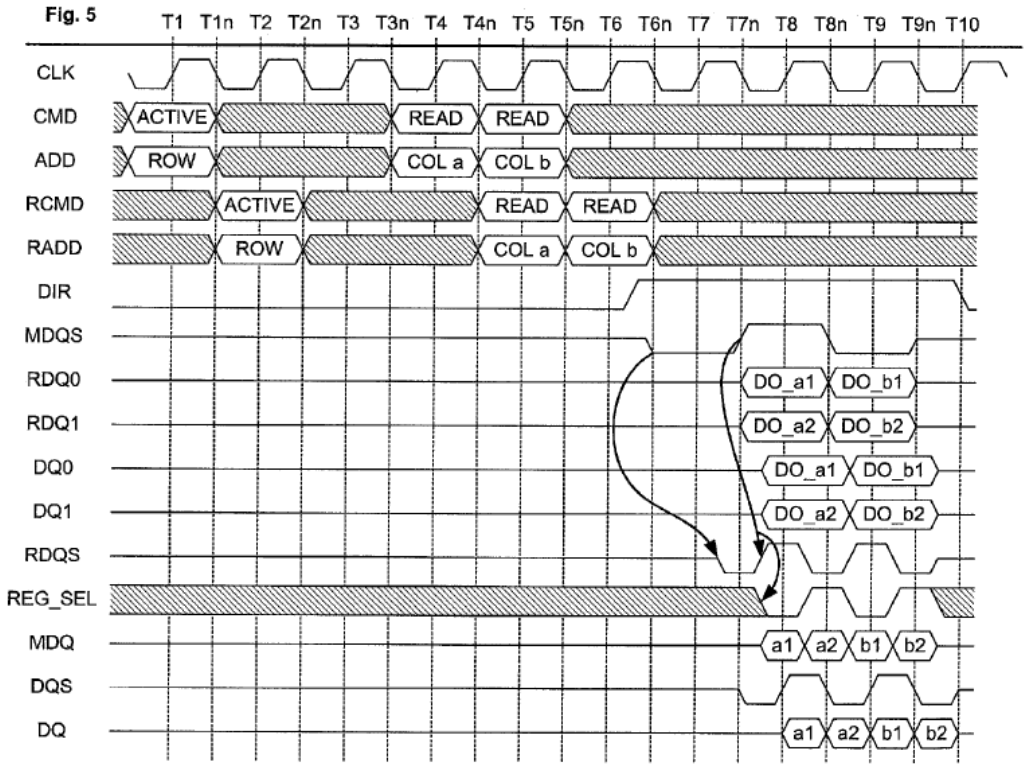
a. Limitation [29.1]

Claim 29 depends on claim 28. Halbert discloses Limitation [29.1] for the same reasons discussed above for Limitation [17.1]. *See* §V.B.3.a; Decl., ¶¶ 394-395.

b. Limitation [29.2]

Halbert discloses Limitation [29.2]. Control DIR enables the set of signal paths for receiving data from the memory array. "When DIR is set to AWAY, buffer 122 is configured as a driver, MUX/DeMUX 124 is configured as a MUX, and registers 126 and 128 are configured as receivers." Halbert, [0034]. Fig. 5 shows that control signal DIR enables a set of signal paths in data interface circuit 120 before the first data bit of the set of consecutively transmitted data bits is transferred through the circuitry (which happens shortly after T7n), i.e., at a quarter clock cycle after T6 (which is before T7n), and disables the set of signal paths after the last data

bit of the set of consecutively transmitted data bits is transferred through the circuitry (which happens shortly after T8n), i.e., at T10 (which is after T8n).



Halbert, Fig. 5; Decl., ¶ 396.

15. Claim 30

a. Limitation [30.1]

Claim 30 depends on claim 28. Halbert discloses Limitation [30.1] for the same reasons discussed above for Limitation [25.1], where the subsequent set of input address and control signals, subsequent write memory command, and subsequent set of registered address and control signals recited in Limitation [30.1] are the second set of input address and control signals, second write memory

command, and second set of registered address and control signals recited in Limitation [25.1], respectively. *See* §V.B.10.a; Decl., ¶¶ 398-400.

b. Limitation [30.2]

Halbert discloses Limitation [30.2] for the same reasons discussed above for Limitation [25.2], where the subsequent set of input address and control signals and subsequent plurality of input chip select signals recited in Limitation [30.2] are the second set of input address and control signals and second plurality of input chip select signals recited in Limitation [25.2], respectively. *See* §V.B.10.b; Decl., ¶¶ 401-404.

c. Limitation [30.3]

Halbert discloses Limitation [30.3] for the same reasons discussed above for Limitation [25.3], where the subsequent set of registered address and control signals, subsequent plurality of registered chip select signals, and subsequent plurality of input chip select signals recited in Limitation [30.3] are the second set of registered address and control signals, second plurality of registered chip select signals, and second plurality of input chip select signals recited in Limitation [25.3], respectively. *See* §V.B.10.c; Decl., ¶¶ 405-408.

d. Limitation [30.4]

Halbert discloses Limitation [30.4] for the same reasons discussed above for Limitation [25.4], where the subsequently registered chip select signal having the active signal value and one or more other subsequently registered chip select signals

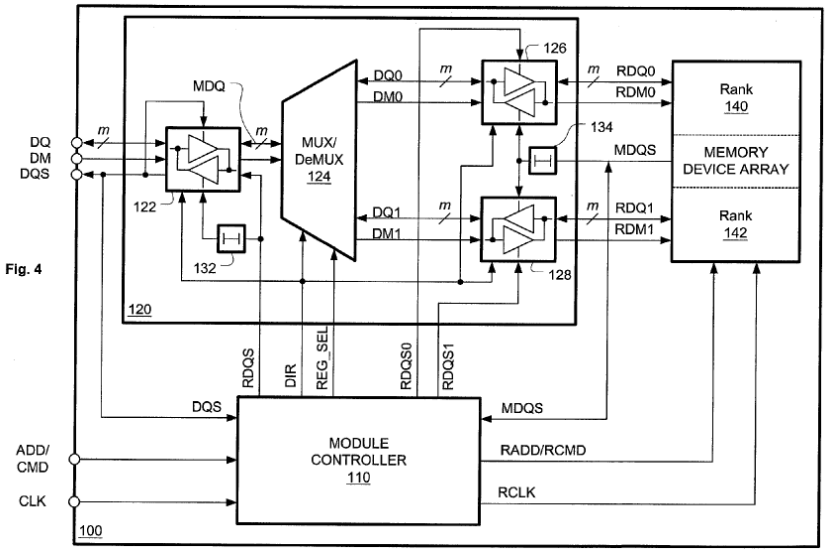
each having the non-active signal value recited in Limitation [30.4] are the second registered chip select signal having the active signal value and one or more other registered chip select signals each having the non-active signal value recited in Limitation [25.4], respectively. *See* §V.B.10.d; Decl., ¶¶ 409-410.

e. Limitation [30.5]

Halbert discloses Limitation [30.5] for the same reasons discussed above for Limitation [25.5], where the subsequently registered chip select signal having the active signal value and subsequent write command recited in Limitation [30.5] are the second registered chip select signal having the active signal value and second write command recited in Limitation [25.5], respectively. *See* §V.B.10.e; Decl., ¶¶ 411-413.

f. Limitation [30.6]

Halbert discloses Limitation [30.6]. As depicted in Fig. 4, shown below, Halbert discloses registers 126, 128, and 122 for providing registered data transfers through data interface circuit 120. Register 128 provides the registered data transfers of the second burst of N-bit wide data signals and the second burst of data strobes between the second rank, i.e., memory device rank 142, and the memory bus 22 through circuit 120.



Halbert, Fig. 4; Decl., ¶ 414. The registered data transfers are in response to the subsequent write command. "[W]hen the module is writing to the memory device array, data signals MDQ from buffer 122 can be channeled to … DQ1." Halbert, [0033]; *see also id*., [0036] ("In the TO mode, REG_SEL determines which of registers 126 and 128 will receive DQ at each memory bus clock cycle."); Fig. 6 (showing WRITE on the CMD line); Decl., ¶ 414.

16. Claim 31

Claim 31 depends on claim 28. Halbert discloses the limitation of Claim 31 for the same reasons discussed above for Claim 22. *See* §V.B.7; Decl., ¶¶ 416-419.

17. Claim 32

a. Limitation [32.1]

Claim 32 depends on claim 28. Halbert discloses Limitation [32.1] for the same reasons discussed above for Limitation [23.1]. *See* §V.B.8.a; Decl., ¶¶ 420-422.

b. Limitation [32.2]

Halbert discloses Limitation [32.2] for the same reasons discussed above for Limitation [23.2]. *See* §V.B.8.b; Decl., ¶ 423.

18. Claim 33

a. Limitation [33.1]

Claim 33 depends on claim 32. Halbert discloses Limitation [33.1] for the same reasons discussed above for Limitation [24.1]. *See* §V.B.9.a; Decl., ¶¶ 425-426.

b. Limitation [33.2]

Halbert discloses Limitation [33.2] for the same reasons discussed above for Limitation [24.2]. *See* §V.B.9.b; Decl., ¶¶ 427-428.

C. No Secondary Considerations Exist

The combination of Halbert in view of JESD21-C would have rendered the Challenged Claims of the '314 patent obvious. No secondary indicia of non-obviousness having a nexus to the putative "invention" of these claims exists contrary to that conclusion. Petitioners reserve their right to respond to any assertion of secondary indicia of nonobviousness advanced by Patent Owner.

VI. The Parallel District Court Case Does Not Warrant Denying Institution

When considering a parallel proceeding, the PTAB "balance[s] considerations such as system efficiency, fairness, and patent quality" using the six factors set forth by the Board in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 5 (PTAB Mar.

20, 2020) (precedential). These factors "overlap," and a "holistic view" should be taken. *Id.*, 6.

The fourth factor (overlap) strongly favors institution. Petitioners have stipulated that they will not pursue invalidity on the same grounds—or even the same references—if the Board institutes trial in this proceeding. Ex. 1010. Petitioners modeled this stipulation on one the Board found to "mitigate any concerns" in *VMware, Inc. v. Intellectual Ventures I LLC*, IPR2020- 00470, Paper 13 at 20 (P.T.A.B. August 18, 2020). This fourth factor favors institution here even more so than in *Apple, Inc. v. SEVEN Networks, LLC*, IPR2020-00156, Paper 10 (P.T.A.B. June 15, 2020). There, the petitioner provided no stipulation. *Id.*, 16-19. Nevertheless, the fourth factor "strongly favored" petitioner. *Id.*

The third factor (investment in parallel proceeding) also favors institution. The district court has not issued any substantive opinions regarding the scope or validity of the Challenged Claims, and given Petitioners' stipulations, the Court is unlikely to invest any resources on the grounds raised in this Petition, either before or after the scheduled institution date. Furthermore, the parallel proceeding is in an early stage, fact discovery has not yet opened, and no trial date has been set. Only initial contentions and claim construction briefs have been exchanged. Ex. 1011.

Regarding the sixth factor (merits, other circumstances), the merits strongly weigh in favor of instituting trial as shown through the strength of the grounds in

this Petition. Other circumstances also favor institution. Like in *Apple v. SEVEN*, the parallel litigation is complex, involving substantial litigation and IPR history regarding the family of patents associated with the '314 patent, three patents, 37 asserted claims, and many accused products. *SEVEN*, 21-22. An IPR trial, in contrast, allows a focus on resolving all Challenged Claims in a single patent, thus "enhanc[ing] the integrity of the patent system." *SEVEN*, 22.

Fintiv factors 1 (stay) and 2 (proximity of trial dates) favor institution. The Court has not yet set the trial date and the related litigation is currently stayed other than claim construction. With the case currently stayed, the Board should consider these two factors "weigh[ing] strongly against exercising [PTAB's] discretion to deny institution." *Shure Inc. v. Clearone, Inc.*, PGR2020-00079, Paper 14 at 15–16, (February 16, 2021) ("In any case, unlike in the NHK and Fintiv cases, there is no trial date set in the Illinois case. Thus, this factor weighs strongly against exercising our discretion to deny the Petition.").

For these reasons, the Board should not exercise its discretion to deny institution of this Petition.

VII. Discretionary Denial Under § 325(d) Is Not Warranted

Advanced Bionics and § 325(d) do not support discretionary denial. The Board's precedential decision in *Advanced Bionics* establishes a two-part framework for evaluating discretionary denial under § 325(d). *Advanced Bionics, LLC v. MED-*

EL Elektromedizinische Geräte GmbH, IPR2019-01469, Paper 6, 8 (PTAB Feb. 13, 2020) (precedential).[4]

As to the second prong, the Examiner "erred in a manner material to the patentability of challenged claims" by overlooking the relevance of Halbert and JESD21-C (the "Asserted Art") against the Challenged Claims of the '314 patent, as shown below. *Advanced Bionics*, IPR2019-01469, Paper 6, 8.

Becton, Dickinson factor c favors institution. The "extent to which the asserted art was evaluated during examination" is nil because the Examiner did not issue a single rejection, much less one where the Asserted Art "was the basis for rejection." *Id.*, 9 n.10. Rather than issuing even a single rejection, the first action on the merits by the Examiner was a Notice of Allowance. Ex. 1002, 210. And even there, the Examiner failed to mention or comment on the Asserted Art—even at a cursory level. *Id.*

Becton, Dickinson factor e favors institution. As shown in the grounds of this Petition, the Asserted Art renders the Challenged Claims obvious. Yet, as noted

[4] The Board noted that the six *Becton, Dickinson* factors a-f are helpful in guiding the two-pronged analysis under *Advanced Bionics*, with factors a, b, and d relevant to the first prong of the *Advanced Bionics* framework, and factors c, e, and f relevant to the second prong. *Advanced Bionics*, IPR2019-01469, Paper 6, 9-11.

above, the Examiner never commented on the Asserted Art's relevance, much less issue a rejection based on them. As such, the Examiner clearly overlooked their relevance. Such human error/oversight in overlooking their relevance is understandable since Patent Owner submitted hundreds of references in numerous IDS's to the Office. Ex. 1002, 164-203. Nonetheless, the Board in *Advanced Bionics* made clear that even such oversight is still one clear example of material error that would preclude discretionary denial under § 325(d). *Advanced Bionics*, IPR2019-01469, Paper 6, 8 n.9 ("An example of a material error may include . . . overlooking specific teachings of the relevant prior art where those teachings impact patentability of the challenged claims"); *id.*, 10 ("[I]f the record of the Office's previous consideration of the art is not well developed or ***silent***, then a petitioner may show the Office erred by overlooking something persuasive under factors (e) and (f)."") (emphasis added).

The Examiner's material error—overlooking specific teachings of relevant prior art—is even more evident considering that the Board in IPR2017-00549 relied upon Halbert to find similar challenged claims in a similar patent in the '314 patent's extended family unpatentable, and the Board in IPR2014-00883, IPR2015-01021, and IPR2015-01020 relied upon JESD21-C to find claims in other patents in the '314 patent's extended family unpatentable. *See supra*, § III(D). Thus, what is clear is that when Halbert and JESD21-C have been substantively considered when

evaluating the patentability of patents in the '314 patent's extended family, the result is claims have been found unpatentable. As shown in the grounds of this Petition, the Challenged Claims are unpatentable. Considering the foregoing, the Examiner made a material error during prosecution that warrants institution.

Becton, Dickinson factor f favors institution. This Petition presents, along with the Asserted Art, the declaration of Dr. Oklobdzija that elaborates on how the teachings of the Asserted Art renders obvious the Challenged Claims. Petitioner submits that the Patent Office would have found the Challenged Claims unpatentable as obvious over the Asserted Art had Dr. Oklobdzija's declaration also been before the Office during prosecution.

As shown, the Asserted Art renders the Challenged Claims unpatentable as obvious, and the strength of the Petition alone supports the Board not exercising its discretion under § 325(d). *See, e.g.*, *Apple, Inc. v. Omni MedSci, Inc.*, IPR2020-00029, Paper 7, 8 (P.T.A.B. Apr. 22, 2020) (finding that "reasonable minds cannot disagree that the Office erred in a manner material to patentability in its treatment of the art by failing to reject the claims … over the references cited in Petitioner's challenges."). The Examiner's material error, detailed above, cements Petitioner's position that discretionary denial of institution under § 325(d) is not warranted. *Advanced Bionics*, IPR2019-01469, Paper 6, 8 n.9.

For at least the foregoing reasons, discretionary denial of institution under § 325(d) is not warranted.

VIII. Mandatory Notices

A. Real Parties-in-Interest

The named Petitioners are the only entities who are funding and controlling this Petition and are therefore all named as real parties-in-interest. No other entity is funding, controlling, or otherwise has an opportunity to control or direct this Petition or Petitioners' participation in any resulting IPR.

B. Related Proceedings

Netlist originally asserted the '314 patent against Petitioners in the Western District of Texas (Waco Division), Case No. 6:21-cv-00431. The case has been transferred to the Western District of Texas (Austin Division), Case No. 1:22-cv-00136-LY.

Petitioners have concurrently filed a second petition challenging different claims of the '314 patent that Netlist has asserted against Petitioners. This Petition challenges claims 15-20 and 22-33, and IPR2022-00744 challenges claims 1-3, 5-6, 8-10, and 12-14.

C. Lead and Backup Counsel

Petitioners' lead and backup counsel are:

Lead Counsel for Petitioner	Backup Counsel for Petitioner
Juan C. Yaquian	Michael Rueckheim

Lead Counsel for Petitioner	Backup Counsel for Petitioner
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D. Electronic Service

Petitioners consent to electronic service at:

Winston-IPR-NetList@winston.com

IX. Fees

The required fee is being paid electronically through PTAB E2E.

X. Conclusion

Petitioners respectfully request that the Board institute IPR and enter a final written decision finding the Challenged Claims unpatentable.

Dated: March 30, 2022

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

This Petition complies with the word count limits set forth in 37 C.F.R. § 42.24(a)(1)(i), because this Petition contains 13,871 words, excluding the parts of the Petition exempted by 37 C.F.R. § 42.24(a)(1) and determined using the word count provided by Microsoft Word, which was used to prepare this Petition.

Dated: March 30, 2022

Respectfully submitted,

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CERTIFICATE OF SERVICE

Under 37 C.F.R. §§ 42.6(e) and 42.105(a), this is to certify that on March 30, 2022, I caused to be served a true and correct copy of the foregoing "**PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 10,489,314**" and Exhibits 1001-1011 by Federal Express on the Patent Owner at the correspondence address of record for U.S. Patent No. 10,489,314:

USCH Law, PC
3790 El Camino Real #1147
Palo Alto CA 94304

A courtesy copy of this Petition and supporting material was also served on litigation counsel for Patent Owner via email:

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